

PICMG 1.3

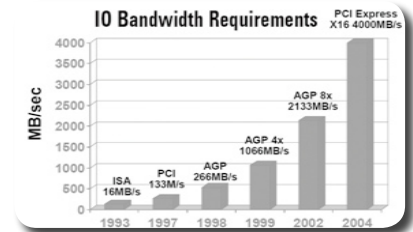
Allows users to protect their investment in PCI (PCI-X) technology while taking advantage of the speed and increased bandwidth of PCI Express

What is PICMG1.3 ?

- **Bring PCI Express to SBC with high speed and bandwidth**
Designed to interface with PCI Express peripherals on a backplane. The PCI Express interconnects with the backplane can operate at x1, x4, x8, x16, and others depending on the capabilities of both the SHB and the backplane.
- **Support PCI(PCI-X) on board with flexibility**
The optional PCI(-X) portion of the SHB interconnect with the backplane allows for 32-bit Operation. The clock rate can be 33MHz, 66MHz, 100MHz, and 133MHz, depending on how the backplane and SHB are designed.
- **Miscellaneous IO**
SATA, USB, IPMB, SMBUS, Geographic Addressing, and PCI wake up to the backplane is specified. Simplified the cabling on SHB for system

PICMG1.3 Key Features

- **PCI Express**
20 PCI Express lanes including x16, x4 and x1 PCI Express configuration are supported
- **Reset signal line defined**
Common header defined on backplane for reset function
- **ATX power signals are supported**
AUX voltages for stand-by power and sleep states (Soft starts, wake-on-LAN)PSON#, PWRGD, PWRRBT#, and ACPI States Supported



So Why PICMG1.3 ?

- The new technology is expected to allow the PCIe transmission rates to keep pace with processor and I/O advances for the next 10 years or more.
- Same basic mechanical dimensions are maintained to minimize chassis redesign expense
- Better host board power management and simplified I/O cabling
- Support PCI Express, PCI option cards without driver changing

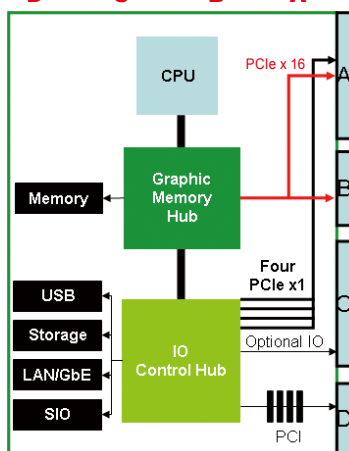
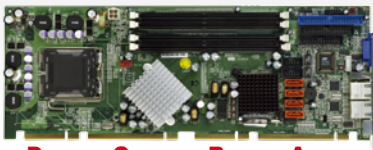
The Future will be.... Chipsets no longer offer native support for ISA

- Faster chipsets & system busses
- Faster CPU
- Chipsets are migrating toward PCI Express



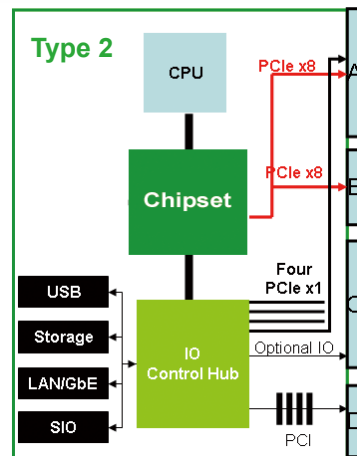
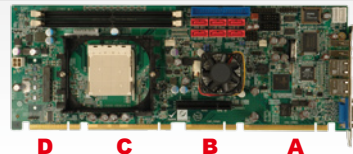
Graphic & Server Grade PICMG 1.3 Solutions

Type 1: Graphic Grade SBC



Support PCIe x16 Graphic Card

Type 2: Server Grade SBC



Support Dual PCIe x8 Application

PICMG1.3 PCIE Slots Configuration

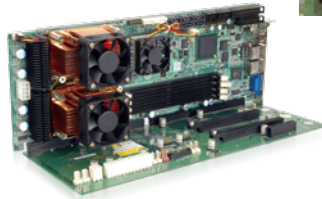
PCIE Slots Available (Non -switch)	SBC Type	Type 1 Graphic Grade		Type 2 Server Grade		
		A	B	A	B	C
		x16	1	1	-	-
x8	x	x	2	2	-	
x4	1	-	1	-	5	
x1	-	4	-	4	-	
Backplane Solution		IEI PE/PXE series		IEI SPE/SPXE series		

Server Grade Intel® 5100 : Optimized performance/watt for ≤200W full size SBC and dense-tiny systems

Intel® 5100 Chipset

IEI Solution

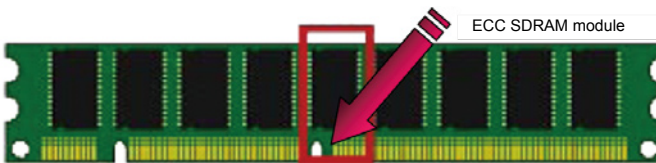
- SPCIE-5100P for Intel® 45nm Mobile Core™ 2 Duo CPU (Penryn)
- SPCIE-5100DX for two way Intel® Xeon® CPU



What is ECC ?

ECC (Error Checking and Correcting) is a kind of parity checking on memory module which can detect both single-bit and multi-bit errors, and will actually correct single-bit errors. ECC requires Parity Memory Module and a setting in the BIOS to be enabled.

Extra Memory Chip for ECC (un-buffered)

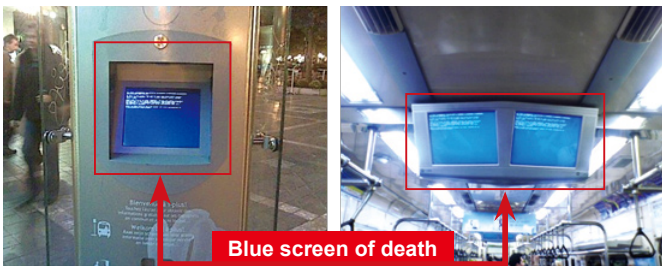


Extra memory chip for ECC (un-buffered)

Why we need ECC ?

ECC has the ability to correct a detected single-bit error in memory. System will continue without a hiccup and even have no idea that anything even happened when ECC has corrected a single-bit error. That is why ECC Memory are predominantly used in servers rather than in client computers.

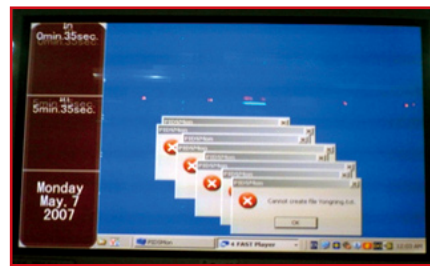
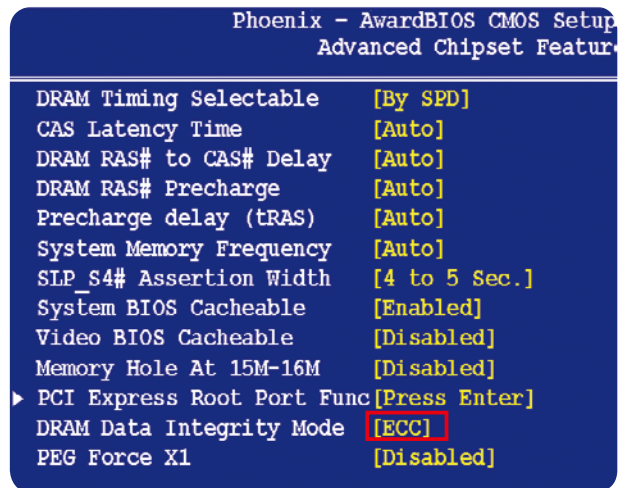
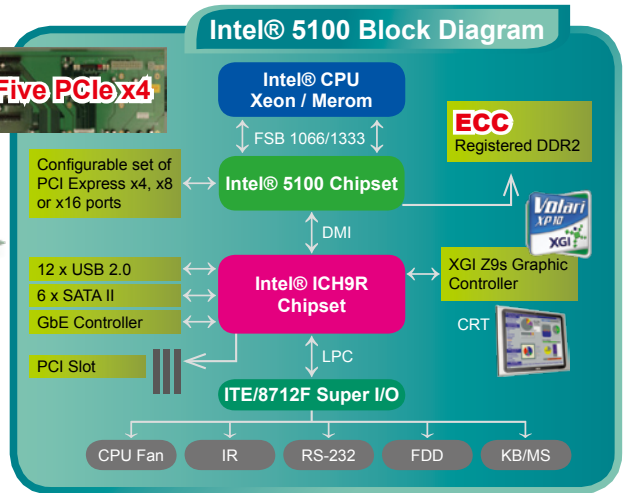
Benefit and Application



Blue screen of death

Reduce system unstable caused by

- ▶ Long-term Operating
- ▶ Heavy Data Loading
- ▶ Complicated Computing



ECC Benefit:

Enhance System Reliability & Security



Industrial Server



ATM (Banking)



Ticket Payment Machine

1

Industrial Computing Solutions

2

Embedded Computing Solutions

3

Industrial Data Collector and Controller

4

Video Capture Solutions

5

I/O Communication Solutions

6

Panel Solutions

7

ORing Network Communication

8

Power Supply Peripherals