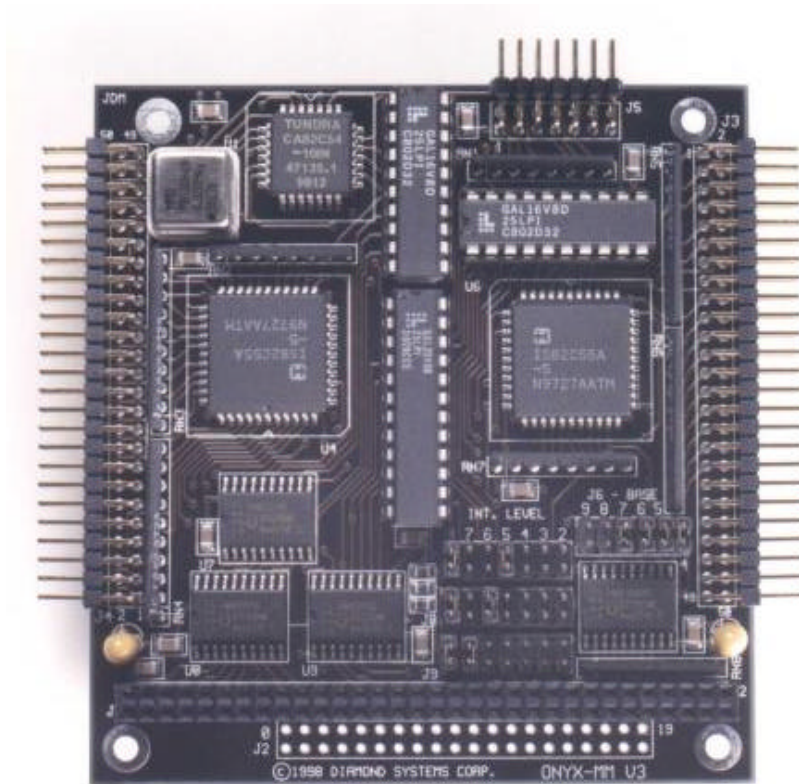




DIAMOND SYSTEMS CORPORATION

ONYX-MM-XT

PC/104 Format
Counter/Timer & Digital I/O Module
User Manual V1.4



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1. General Information and Features

ONYX-MM is a PC/104-compliant I/O module with 48 digital I/O lines, 3 16-bit counter/timers, and 3 interrupts. It is an 8-bit module, so it does not contain the 16-bit expansion bus connector. This connector is available as an option by requesting the -B16 suffix when ordering.

Three right-angle pin headers are provided for I/O. Two identical 50-pin (2x25) headers contain 24 digital I/O lines each and +5/ground, and a third 14-pin (2x7) header provides the counter/timer signals, external interrupt pin, and +5/ground. J2, with 24 digital I/O lines, is on the right side of the module in the standard PC/104 I/O position. J3, with 24 additional digital I/O lines, is on the left side of the module, and J4, with the counter/timer and interrupt signals, is on the top edge of the module. (The bottom edge of the module is defined as the edge with the PC/104 ISA bus connectors.)

All I/O signals are TTL compatible.

The boards operate on +5V power supply only.

Digital I/O

48 TTL digital I/O lines are provided by 2 82C55 chips (24 per chip). Each line can source 2.5mA in a logic 0 state and sink 2.5mA in a logic 1 state. I/O lines are unbuffered, i.e. there is a direct connection between the 82C55 and the I/O header. Bit C0 of each 82C55 can be used to generate an interrupt on the PC bus (see **Interrupts** below).

All digital I/O lines are connected to +5V through 10K Ω pull-up resistors.

Digital I/O lines are accessed through two 50-pin headers, J3 and J4, with 24 lines (one 82C55) on each header. See page 8 for I/O header pinouts.

Counter/Timer I/O

Onyx-MM contains three 16-bit counter/timers provided by an 82C54 chip. Each counter/timer has an input pin, a gate pin, and an output pin. The input pin responds to positive edges. The gate pin is active high; a counter will count whenever its associated gate pin is high and will not count when the gate pin is low. The input and gate pins are connected to +5V through 10K Ω pull-up resistors.

Counter/timer I/O lines are accessed through a 14-pin header J5. See page 8 for the pinout of J5.

An on-board oscillator provides a 4MHz clock that can be used to drive any counter. Each counter has a maximum input rate of 10MHz.

Programmable features include input source selection and counter cascading:

Counter 0 input can be either IN0 from the I/O header or 4MHz.

Counter 1 input can be either IN1, 4MHz, or Counter 0 output.

Counter 2 input can be either IN2, 4MHz, or Counter 1 output.

All three counter outputs can be programmed to generate PC bus interrupts as described below. With appropriate configuration, two or three counters can be cascaded to form a 32-bit or 48-bit counter, and the output of this cascaded counter can generate an interrupt.

Interrupts

ONYX-MM provides a means to generate up to three active-high interrupt signals on the PC/104 bus. Three pin headers are provided to select interrupt levels for each interrupt signal. Interrupt levels 2 through 7 are available on each header.

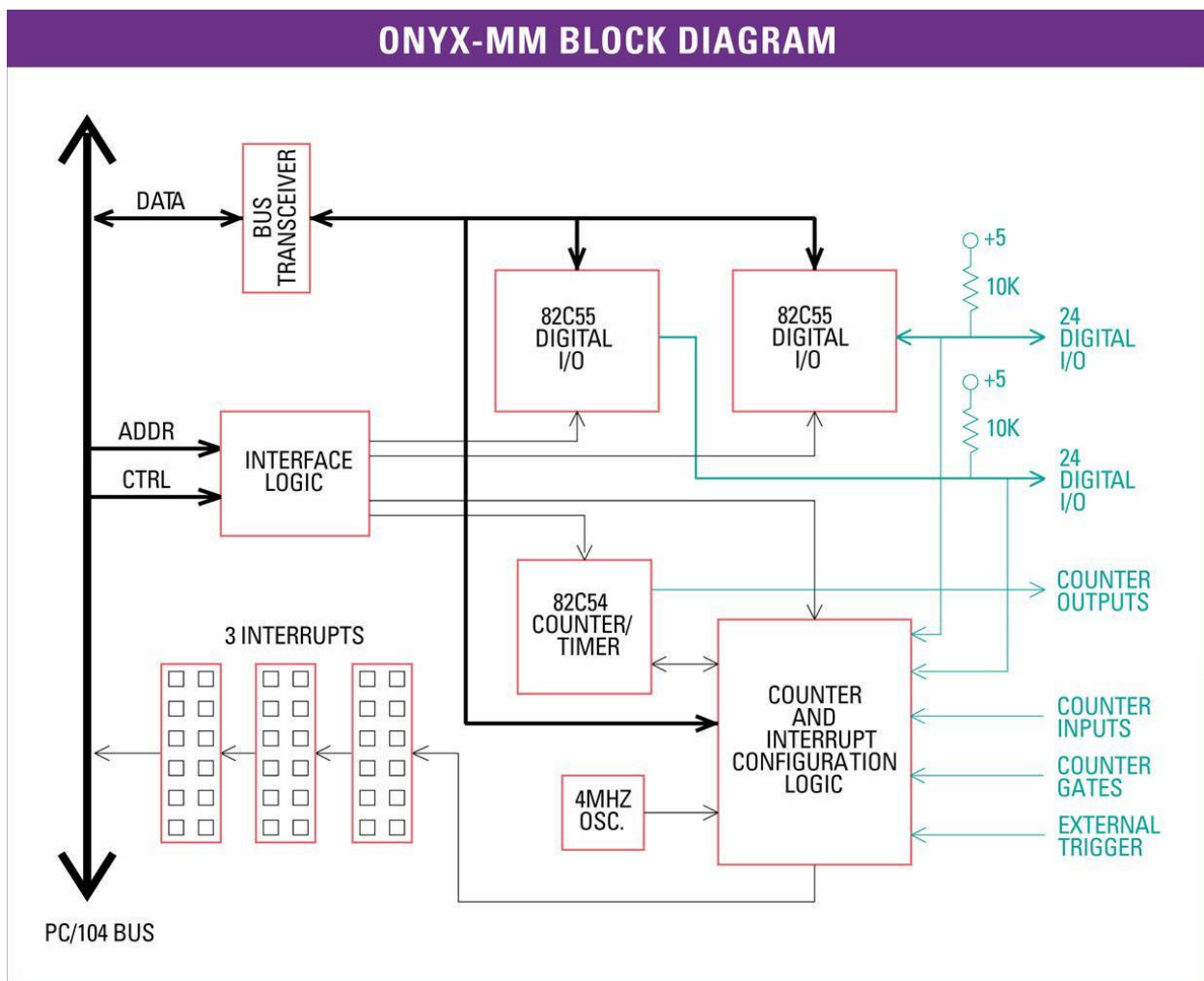
To enable interrupt sharing, a 1K pull-down resistor can be jumpered to each interrupt line, and interrupt signals are driven by tristate drivers. When an interrupt is pending, the interrupt line is driven high, and when it is not pending, the output is in high-impedance mode, and the 1K resistor pulls it down to a logic 0 state.

Interrupt sources are programmable. Interrupts can be generated from both digital I/O and counter/timer signals as follows:

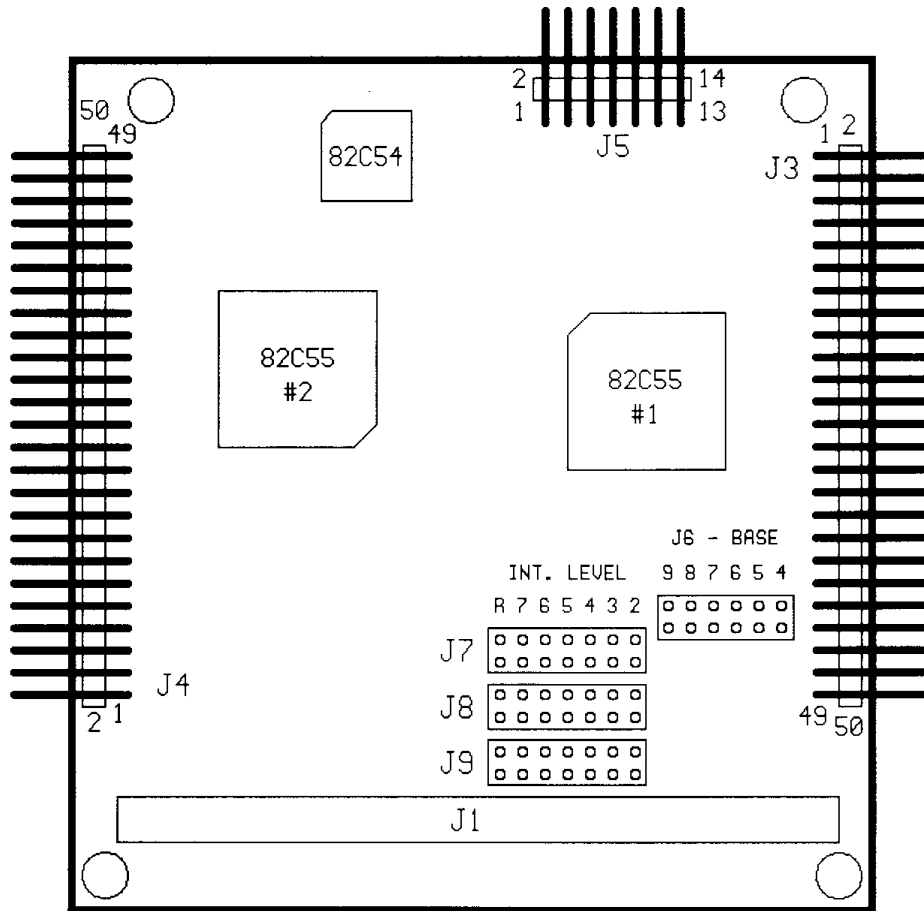
- Interrupt no. 1: Bit C0 from 82C55 #1 or Counter 0 output
- Interrupt no. 2: Bit C0 from 82C55 #2 or Counter 1 output
- Interrupt no. 3: External interrupt pin or Counter 2 output

Interrupts are enabled and disabled under software control by manipulating a control register.

Block Diagram



2. Board Drawing



| Item | Description |
|------|----------------------------------|
| J1 | PC/104 bus connector |
| J3 | Digital I/O ports 1A, 1B, 1C |
| J4 | Digital I/O ports 2A, 2B, 2C |
| J5 | Counter/timer signals |
| J6 | Board base address configuration |
| J7 | Interrupt 0 configuration |
| J8 | Interrupt 1 configuration |
| J9 | Interrupt 2 configuration |

3. I/O Header Pinouts

J3: Digital I/O Header for 82C55 #1

J4: Digital I/O Header for 82C55 #2

Each of these headers is identical in pinout. They provide 24 digital I/O lines, +5, and ground. Pin 1 of J3 is in the upper right corner of the board, and pin 1 of J4 is in the lower left corner.

| | | | |
|----|----|----|-----|
| A7 | 1 | 2 | Gnd |
| A6 | 3 | 4 | Gnd |
| A5 | 5 | 6 | Gnd |
| A4 | 7 | 8 | Gnd |
| A3 | 9 | 10 | Gnd |
| A2 | 11 | 12 | Gnd |
| A1 | 13 | 14 | Gnd |
| A0 | 15 | 16 | Gnd |
| C7 | 17 | 18 | Gnd |
| C6 | 19 | 20 | Gnd |
| C5 | 21 | 22 | Gnd |
| C4 | 23 | 24 | Gnd |
| C3 | 25 | 26 | Gnd |
| C2 | 27 | 28 | Gnd |
| C1 | 29 | 30 | Gnd |
| C0 | 31 | 32 | Gnd |
| B7 | 33 | 34 | Gnd |
| B6 | 35 | 36 | Gnd |
| B5 | 37 | 38 | Gnd |
| B4 | 39 | 40 | Gnd |
| B3 | 41 | 42 | Gnd |
| B2 | 43 | 44 | Gnd |
| B1 | 45 | 46 | Gnd |
| B0 | 47 | 48 | Gnd |
| +5 | 49 | 50 | Gnd |

J5: Counter/Timer and Interrupt Header

This header is a 14-pin header with all counter/timer signals, the external interrupt pin, +5, and ground.

| | | | |
|--------|----|----|--------------------|
| In 0 | 1 | 2 | In 1 |
| Gate 0 | 3 | 4 | Gate 1 |
| Out 0 | 5 | 6 | Out 1 |
| In 2 | 7 | 8 | External Interrupt |
| Gate 2 | 9 | 10 | Gnd |
| Out 2 | 11 | 12 | Gnd |
| +5 | 13 | 14 | Gnd |

4. Base Address Configuration

ONYX-MM's base address is set with header J6, located at the lower right corner of the board. Each of the six pairs of pins on J6 corresponds to a different address bit. A pair left open is equal to a 1, and a pair with a jumper installed is equal to a 0. The header is used to select address bits 9-4, resulting in an 16-byte I/O decode. The leftmost pair selects address bit A9, and the rightmost pair selects address bit A4. Although any 16-byte location is selectable, certain locations are reserved or may cause conflicts. The table below lists recommended base address settings for ONYX-MM. The default setting is 300 Hex. "Open" means an open position, and "Inst" means a position with a jumper installed.

| Base Address | | Header J6 Position | | | | | |
|--------------|---------------|--------------------|------|------|------|------|------|
| Hex | Decimal | 9 | 8 | 7 | 6 | 5 | 4 |
| 220 | 544 | Open | Inst | Inst | Inst | Open | Inst |
| 240 | 576 | Open | Inst | Inst | Open | Inst | Inst |
| 250 | 592 | Open | Inst | Inst | Open | Inst | Open |
| 260 | 608 | Open | Inst | Inst | Open | Open | Inst |
| 280 | 640 | Open | Inst | Open | Inst | Inst | Inst |
| 290 | 656 | Open | Inst | Open | Inst | Inst | Open |
| 2A0 | 672 | Open | Inst | Open | Inst | Open | Inst |
| 2B0 | 688 | Open | Inst | Open | Inst | Open | Open |
| 2C0 | 704 | Open | Inst | Open | Open | Inst | Inst |
| 2D0 | 720 | Open | Inst | Open | Open | Inst | Open |
| 2E0 | 736 | Open | Inst | Open | Open | Open | Inst |
| 300 | 768 (Default) | Open | Open | Inst | Inst | Inst | Inst |
| 330 | 816 | Open | Open | Inst | Inst | Open | Open |
| 340 | 832 | Open | Open | Inst | Open | Inst | Inst |
| 350 | 848 | Open | Open | Inst | Open | Inst | Open |
| 360 | 864 | Open | Open | Inst | Open | Open | Inst |
| 380 | 896 | Open | Open | Open | Inst | Inst | Inst |
| 390 | 912 | Open | Open | Open | Inst | Inst | Open |
| 3A0 | 928 | Open | Open | Open | Inst | Open | Inst |
| 3C0 | 960 | Open | Open | Open | Open | Inst | Inst |
| 3E0 | 992 | Open | Open | Open | Open | Open | Inst |

5. Interrupt Configuration

Each interrupt signal has its own configuration jumper block. The jumper block configures the interrupt level and the 1K Ohm pull-down resistor. A pull-down resistor is required on each active interrupt line on the PC/104 bus. Only one resistor should be installed per interrupt level for the entire system.

J7: Interrupt #0

J8: Interrupt #1

J9: Interrupt #2

| Position | Function | Open | Jumper |
|-----------------|-----------------|--|----------------------------|
| R | 1K Ohm Resistor | No pulldown | Pulldown (max 1 per level) |
| 7 | IRQ7 | | |
| 6 | IRQ6 | Install only one jumper in each header in any of these 6 locations to select the interrupt level | |
| 5 | IRQ5 | | |
| 4 | IRQ4 | | |
| 3 | IRQ3 | | |
| 2 | IRQ2 | | |

All three interrupt sources can be set to the same level if desired. However only one pulldown resistor should be installed for each interrupt level.

6. Register Map

| Base + | Function | Comments |
|---------------|--|------------------------------|
| 0 | DIO port 1A | 0 - 3 are 82C55 #1 registers |
| 1 | DIO port 1B | |
| 2 | DIO port 1C | |
| 3 | DIO port 1 configuration register | |
| 4 | DIO port 2A | 4 - 7 are 82C55 #2 registers |
| 5 | DIO port 2B | |
| 6 | DIO port 2C | |
| 7 | DIO port 2 configuration register | |
| 8 | Counter/timer 0 data | 8 - 11 are 82C54 registers |
| 9 | Counter/timer 1 data | |
| 10 | Counter/timer 2 data | |
| 11 | Counter/timer mode configuration register | |
| 12 | Counter/timer input configuration register | |
| 13 | (maps to register 12) | |
| 14 | Interrupt configuration register | |
| 15 | (maps to register 14) | |

Note that locations 12 and 13 both map to the same physical register on Onyx-MM. Likewise locations 14 and 15 both map to the same physical register on the board.

7. Register definitions

Base + 0: Digital I/O Register A, 82C55 no. 1

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 1A7 | 1A6 | 1A5 | 1A4 | 1A3 | 1A2 | 1A1 | 1A0 |

1A7-1A0 Digital I/O port 1A, port A on 82C55 no. 1

Base + 1: Digital I/O Register B, 82C55 no. 1

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 1B7 | 1B6 | 1B5 | 1B4 | 1B3 | 1B2 | 1B1 | 1B0 |

1B7-1B0 Digital I/O port 1B, port B on 82C55 no. 1

Base + 2: Digital I/O Register C, 82C55 no. 1

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 1C7 | 1C6 | 1C5 | 1C4 | 1C3 | 1C2 | 1C1 | 1C0 |

1C7-1C0 Digital I/O port 1C, port C on 82C55 no. 1

Base + 4: Digital I/O Register A, 82C55 no. 2

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 2A7 | 2A6 | 2A5 | 2A4 | 2A3 | 2A2 | 2A1 | 2A0 |

2A7-2A0 Digital I/O port 2A, port A on 82C55 no. 2

Base + 5: Digital I/O Register B, 82C55 no. 2

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 2B7 | 2B6 | 2B5 | 2B4 | 2B3 | 2B2 | 2B1 | 2B0 |

2B7-2B0 Digital I/O port 2B, port B on 82C55 no. 2

Base + 6: Digital I/O Register C, 82C55 no. 2

| | | | | | | | | |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 2C7 | 2C6 | 2C5 | 2C4 | 2C3 | 2C2 | 2C1 | 2C0 |

2C7-2C0 Digital I/O port 2C, port C on 82C55 no. 2

Base + 3: Digital I/O Configuration Register, 82C55 no. 1

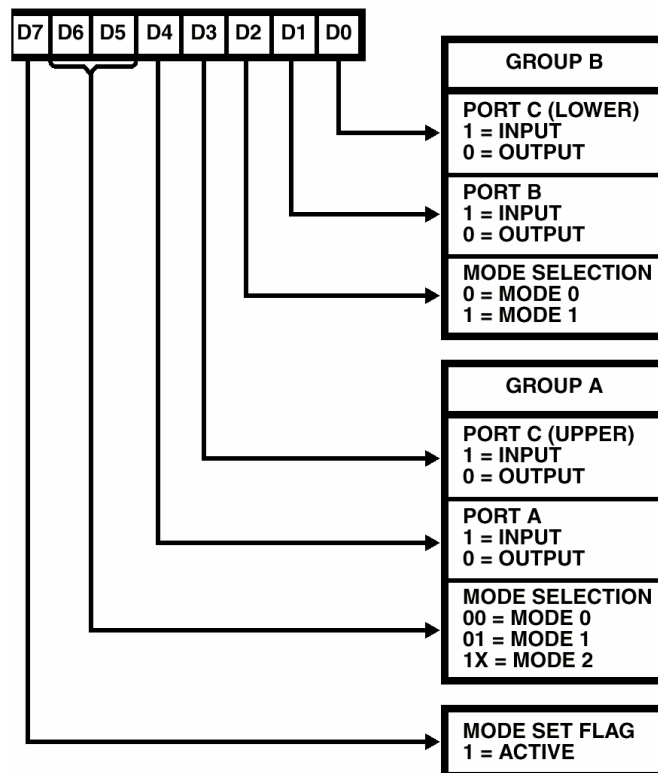
Base + 7: Digital I/O Configuration Register, 82C55 no. 2

These control registers determine the direction and mode of the 82C55 digital I/O lines. The diagram below comes from the 82C55 chip datasheet which is included at the back of this manual. Base + 3 is the control register for chip 1, and Base + 7 is the control register for chip 2.

Most applications use the simple I/O configuration in which bit 7 is set to 1 and the Mode is set to 0 for all ports.

Here is a list of common configuration register control bytes:

| Configuration Byte | | Port A | Port B | Port C (both halves) |
|--------------------|---------|--------|--------|----------------------|
| Hex | Decimal | | | |
| 9B | 155 | Input | Input | Input |
| 92 | 146 | Input | Input | Output |
| 99 | 153 | Input | Output | Input |
| 90 | 144 | Input | Output | Output |
| 8B | 139 | Output | Input | Input |
| 82 | 130 | Output | Input | Output |
| 89 | 137 | Output | Output | Input |
| 80 | 128 | Output | Output | Output |



Base + 8: Counter/Timer 0 Data

| | | | | | | | | |
|------|----|----|----|----|----|----|----|----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

D7-D0 Divisor bits 7-0 or 15-8

Base + 9: Counter/Timer 1 Data

| | | | | | | | | |
|------|----|----|----|----|----|----|----|----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

D7-D0 Divisor bits 7-0 or 15-8

Base + 10: Counter/Timer 2 Data

| | | | | | | | | |
|------|----|----|----|----|----|----|----|----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

D7-D0 Divisor bits 7-0 or 15-8

Base + 11: Counter/Timer Configuration

The diagram below is from the 82C54 datasheet which is included at the back of this manual.

| | | | | | | | |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ |
| SC1 | SC0 | RW1 | RW0 | M2 | M1 | M0 | BCD |

SC — Select Counter:

| SC1 | SC0 | |
|-----|-----|--|
| 0 | 0 | Select Counter 0 |
| 0 | 1 | Select Counter 1 |
| 1 | 0 | Select Counter 2 |
| 1 | 1 | Read-Back Command (See Read Operations) |

M — MODE:

| M2 | M1 | M0 | |
|----|----|----|--------|
| 0 | 0 | 0 | Mode 0 |
| 0 | 0 | 1 | Mode 1 |
| X | 1 | 0 | Mode 2 |
| X | 1 | 1 | Mode 3 |
| 1 | 0 | 0 | Mode 4 |
| 1 | 0 | 1 | Mode 5 |

RW — Read/Write:

| RW1 | RW0 | |
|-----|-----|--|
| 0 | 0 | Counter Latch Command (see Read Operations) |
| 0 | 1 | Read/Write least significant byte only. |
| 1 | 0 | Read/Write most significant byte only. |
| 1 | 1 | Read/Write least significant byte first, then most significant byte. |

BCD:

| | |
|---|---|
| 0 | Binary Counter 16-bits |
| 1 | Binary Coded Decimal (BCD) Counter (4 Decades) |

The registers described below are built in to the Onyx-MM circuitry and are separate from the 82C55 and 82C54 chips. In the register maps below, blank locations are unused. See the accompanying schematic diagrams on the following pages.

Base + 12: Counter/timer input configuration register

| | | | | | | | | |
|------|---|---|---|-----|-----|-----|-----|----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | | | S21 | S20 | S11 | S10 | S0 |

S21 - S20 Counter 2 input select:

| S21 | S20 | Input source |
|-----|-----|-----------------|
| 0 | 0 | In2 |
| 0 | 1 | 4MHz oscillator |
| 1 | X | Out1 |

S11 - S10 Counter 1 input select:

| S11 | S10 | Input source |
|-----|-----|-----------------|
| 0 | 0 | In1 |
| 0 | 1 | 4MHz oscillator |
| 1 | X | Out0 |

S0 Counter 0 input select

| | |
|---|-----------------|
| 0 | In0 |
| 1 | 4MHz oscillator |

Base + 14: Interrupt configuration register

| | | | | | | | | |
|------|---|---|------|------|------|-------|-------|-------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | | SRC2 | SRC1 | SRC0 | INTE2 | INTE1 | INTE0 |

SRC2 Interrupt source 2:

| | |
|---|------------------------|
| 0 | External interrupt pin |
| 1 | Counter 2 output |

SRC1 Interrupt source 1:

| | |
|---|--|
| 0 | Bit C0 from 82C55 #2 (base + 6, bit 0) |
| 1 | Counter 1 output |

SRC0 Interrupt source 0:

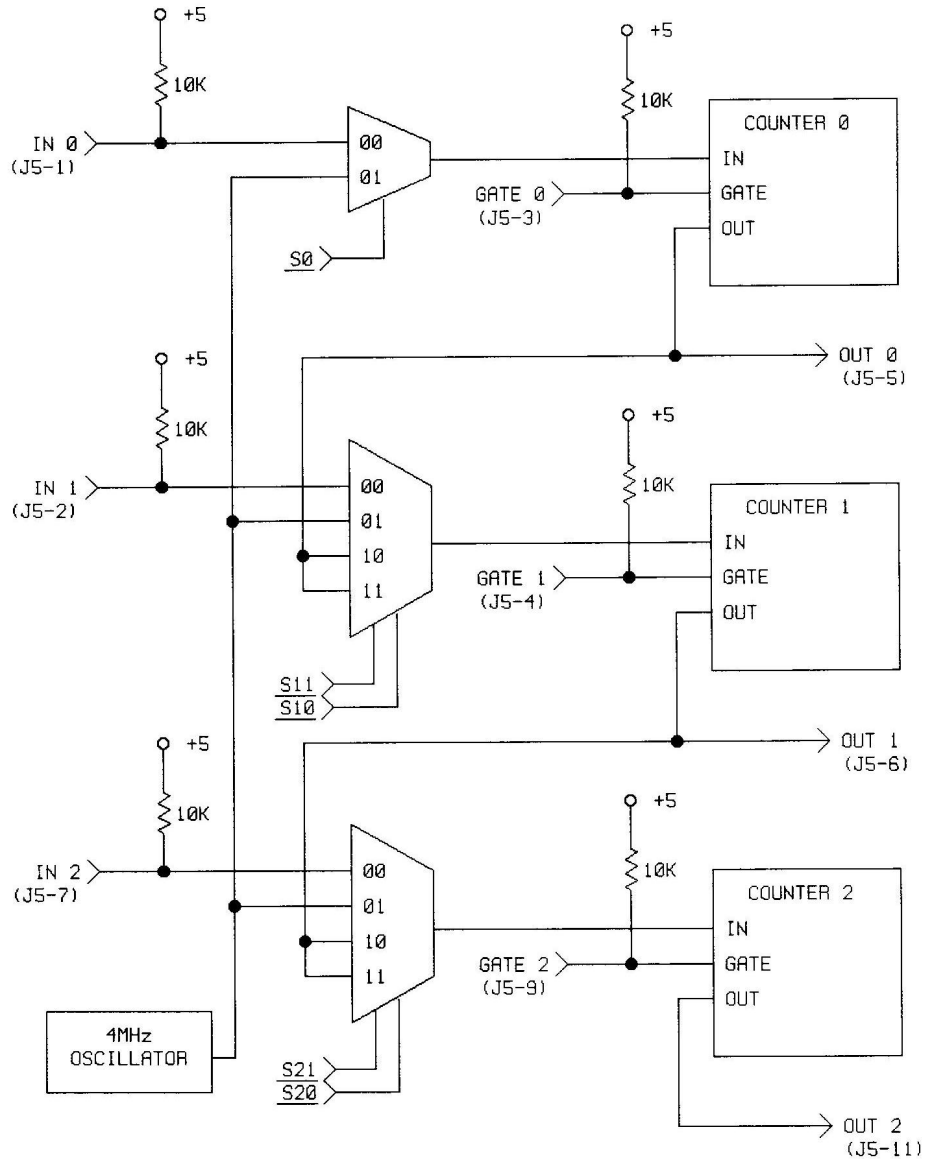
| | |
|---|--|
| 0 | Bit C0 from 82C55 #1 (base + 2, bit 0) |
| 1 | Counter 0 output |

INTE2 - 0 Interrupt enable signals

| | |
|---|----------|
| 0 | Disabled |
| 1 | Enabled |

8. Counter/Timer Circuit Schematic

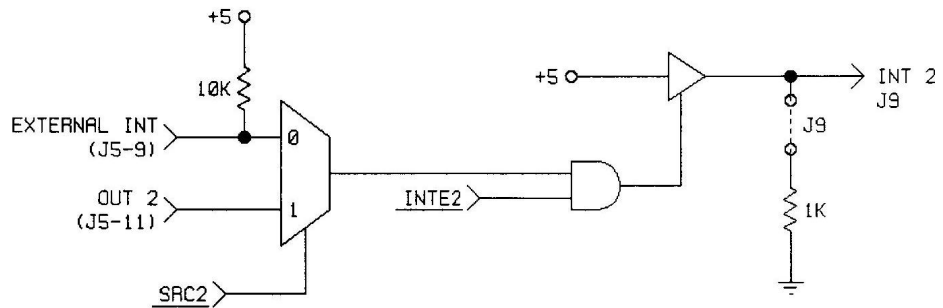
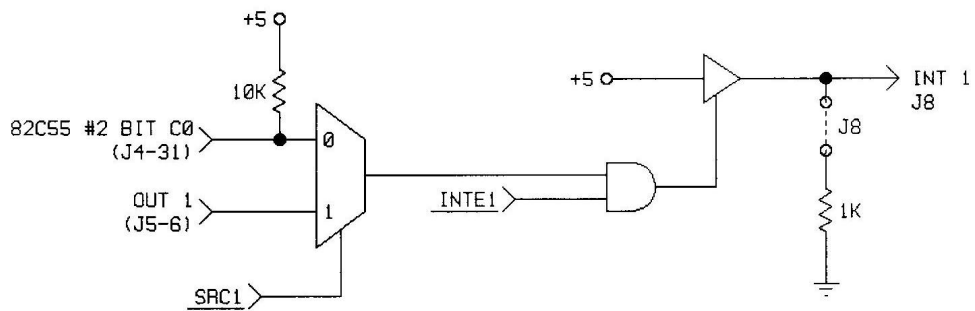
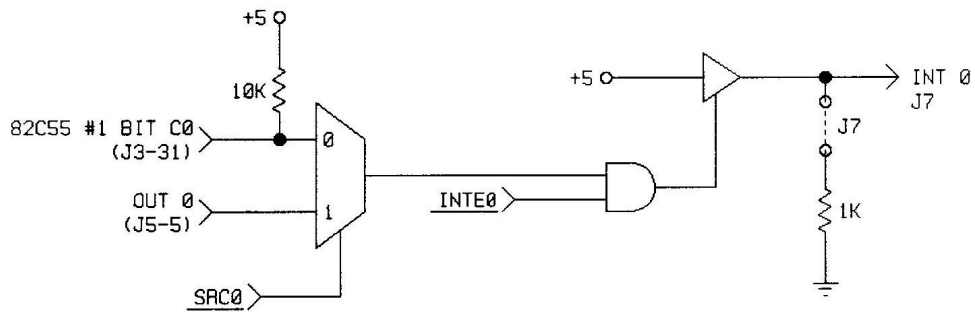
The schematic below illustrates the counter/timer configuration and how the counter/timer input configuration register controls it. See the control register description on page 13.



S20 UNDERLINE INDICATES CONTROL REGISTER BIT
 (J5-11) PARENTHESES INDICATE I/O HEADER AND PIN NO.

9. Interrupt Circuit Schematic

The schematic below illustrates the interrupt circuit configuration and how the interrupt configuration register controls it. See the control register description on page 13.



INTE2 UNDERLINE INDICATES CONTROL REGISTER BIT
 (J5-11) PARENTHESES INDICATE I/O HEADER AND PIN NO.

10. Specifications

Counter/Timer Circuitry

| | |
|------------------------------|----------------------------------|
| Chip | 82C54-2 |
| Counter/timers | 3, 16 bits wide |
| Maximum input frequency | 10MHz |
| On-board oscillator | 4MHz \pm .01% (100 ppm) |
| Signal type | TTL |
| Input voltage, all inputs: | |
| Low | -0.5V min, 0.8V max |
| High | 2.0V min, 5.5V max |
| Input current | -200 A max (low), 2 A max (high) |
| Output voltage, all outputs: | |
| Low | 0.0V min, 0.4V max |
| High | 3.0V min, Vcc - 0.4V max |
| Output current | \pm 2.5mA max, each line |
| Pullup resistors | 10K all input lines |

Digital I/O Circuitry

| | |
|---------------------|---|
| Chip | 82C55A (x2) |
| Number of I/O lines | 48 |
| Direction | All lines programmable for input or output in groups of 4/8 |
| Input voltage: | |
| Low | -0.5V min, 0.8V max |
| High | 2.0V min, 5.5V max |
| Output voltage: | |
| Low | 0.0V min, 0.4V max |
| High | 3.0V min, Vcc - 0.4V max |
| Output current | \pm 2.5mA max, each line |
| Pullup resistors | 10K all lines |

Interrupt Circuitry

| | |
|--------------------|---|
| No. of interrupts | 3 |
| Pull-down resistor | 1K resistor selectable via jumper on each interrupt |
| Interrupt levels | 2 - 7 |

General

| | |
|--------------------|--|
| Dimensions | 3.550" x 3.775" |
| Power supply (Vcc) | 5.0VDC \pm 10%, 200mA typical (all outputs open) |
| Card type | 8-bit PC/104 bus compliant |
| Temperature range | -40 - +85°C, operating and storage |

March 1997

CMOS Programmable Interval Timer

Features

- 8MHz to 12MHz Clock Input Frequency
- Compatible with NMOS 8254
 - Enhanced Version of NMOS 8253
- Three Independent 16-Bit Counters
- Six Programmable Counter Modes
- Status Read Back Command
- Binary or BCD Counting
- Fully TTL Compatible
- Single 5V Power Supply
- Low Power
 - ICCSB10 μ A
 - ICCOP10mA at 8MHz
- Operating Temperature Ranges
 - C82C540 $^{\circ}$ C to +70 $^{\circ}$ C
 - I82C54-40 $^{\circ}$ C to +85 $^{\circ}$ C
 - M82C54-55 $^{\circ}$ C to +125 $^{\circ}$ C

Description

The Harris 82C54 is a high performance CMOS Programmable Interval Timer manufactured using an advanced 2 micron CMOS process.

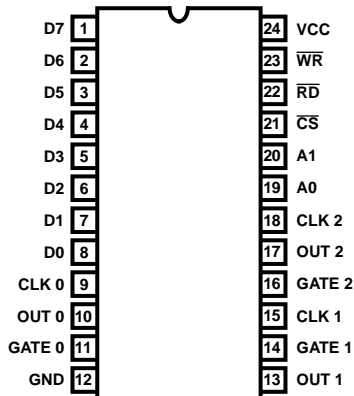
The 82C54 has three independently programmable and functional 16-bit counters, each capable of handling clock input frequencies of up to 8MHz (82C54) or 10MHz (82C54-10) or 12MHz (82C54-12).

The high speed and industry standard configuration of the 82C54 make it compatible with the Harris 80C86, 80C88, and 80C286 CMOS microprocessors along with many other industry standard processors. Six programmable timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, and many other applications. Static CMOS circuit design insures low power operation.

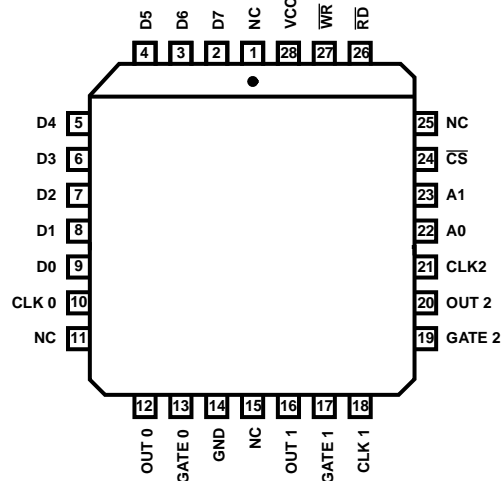
The Harris advanced CMOS process results in a significant reduction in power with performance equal to or greater than existing equivalent products.

Pinouts

82C54 (PDIP, Cerdip, SOIC)
TOP VIEW



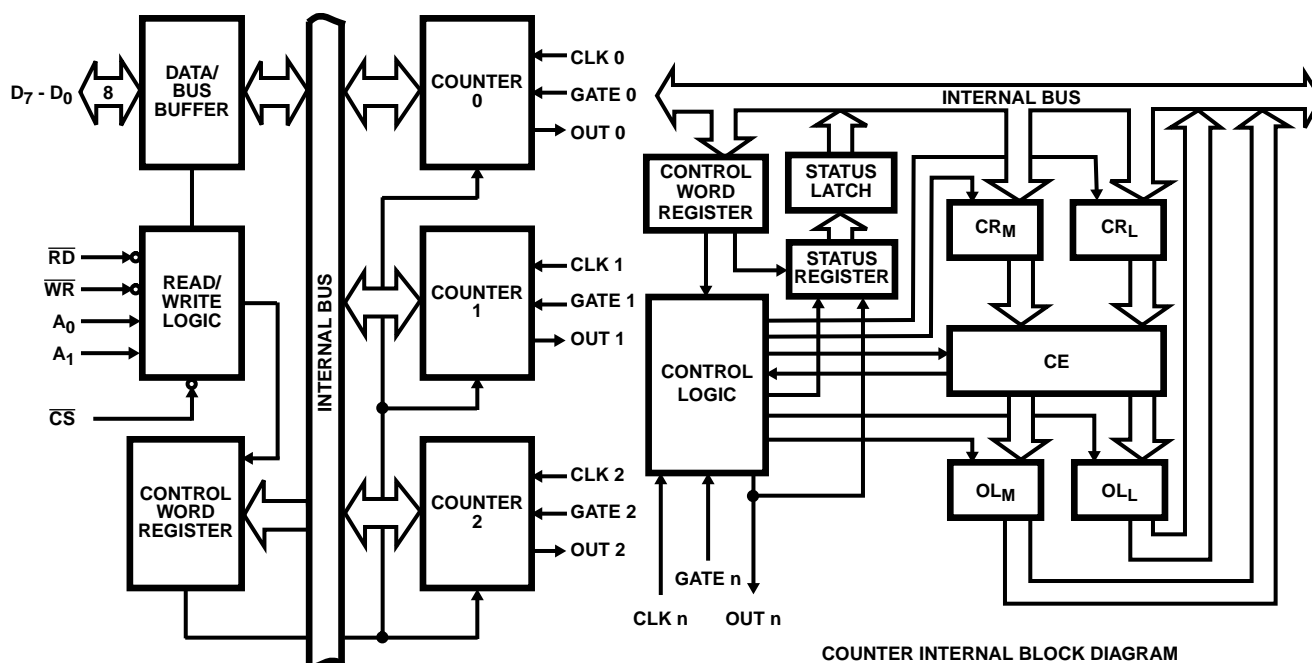
82C54 (PLCC/CLCC)
TOP VIEW



Ordering Information

| PART NUMBERS | | | TEMPERATURE RANGE | PACKAGE | PKG. NO. |
|-----------------|--------------|--------------|-------------------|----------------|----------|
| 8MHz | 10MHz | 12MHz | | | |
| CP82C54 | CP82C54-10 | CP82C54-12 | 0°C to +70°C | 24 Lead PDIP | E24.6 |
| IP82C54 | IP82C54-10 | IP82C54-12 | -40°C to +85°C | 24 Lead PDIP | E24.6 |
| CS82C54 | CS82C54-10 | CS82C54-12 | 0°C to +70°C | 28 Lead PLCC | N28.45 |
| IS82C54 | IS82C54-10 | IS82C54-12 | -40°C to +85°C | 28 Lead PLCC | N28.45 |
| CD82C54 | CD82C54-10 | CD82C54-12 | 0°C to +70°C | 24 Lead CERDIP | F24.6 |
| ID82C54 | ID82C54-10 | ID82C54-12 | -40°C to +85°C | 24 Lead CERDIP | F24.6 |
| MD82C54/B | MD82C54-10/B | MD82C54-12/B | -55°C to +125°C | 24 Lead CERDIP | F24.6 |
| MR82C54/B | MR82C54-10/B | MR82C54-12/B | -55°C to +125°C | 28 Lead CLCC | J28.A |
| SMD # 8406501JA | - | 8406502JA | -55°C to +125°C | 24 Lead CERDIP | F24.6 |
| SMD# 84065013A | - | 84065023A | -55°C to +125°C | 28 Lead CLCC | J28.A |
| CM82C54 | CM82C54-10 | CM82C54-12 | 0°C to +70°C | 24 Lead SOIC | M24.3 |

Functional Diagram



Pin Description

| SYMBOL | DIP PIN NUMBER | TYPE | DEFINITION |
|---------|----------------|------|--|
| D7 - D0 | 1 - 8 | I/O | DATA: Bi-directional three-state data bus lines, connected to system data bus. |
| CLK 0 | 9 | I | CLOCK 0: Clock input of Counter 0. |
| OUT 0 | 10 | O | OUT 0: Output of Counter 0. |
| GATE 0 | 11 | I | GATE 0: Gate input of Counter 0. |
| GND | 12 | | GROUND: Power supply connection. |
| OUT 1 | 13 | O | OUT 1: Output of Counter 1. |
| GATE 1 | 14 | I | GATE 1: Gate input of Counter 1. |
| CLK 1 | 15 | I | CLOCK 1: Clock input of Counter 1. |
| GATE 2 | 16 | I | GATE 2: Gate input of Counter 2. |
| OUT 2 | 17 | O | OUT 2: Output of Counter 2. |

Pin Description (Continued)

| SYMBOL | DIP PIN NUMBER | TYPE | DEFINITION | | | | | | | | | | | | | | | |
|-----------------|----------------|-----------------------|--|----|----|---------|---|---|-----------|---|---|-----------|---|---|-----------|---|---|-----------------------|
| CLK 2 | 18 | I | CLOCK 2: Clock input of Counter 2. | | | | | | | | | | | | | | | |
| A0, A1 | 19 - 20 | I | ADDRESS: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus. <table border="1" data-bbox="548 380 1089 569"> <thead> <tr> <th>A1</th> <th>A0</th> <th>SELECTS</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Counter 0</td> </tr> <tr> <td>0</td> <td>1</td> <td>Counter 1</td> </tr> <tr> <td>1</td> <td>0</td> <td>Counter 2</td> </tr> <tr> <td>1</td> <td>1</td> <td>Control Word Register</td> </tr> </tbody> </table> | A1 | A0 | SELECTS | 0 | 0 | Counter 0 | 0 | 1 | Counter 1 | 1 | 0 | Counter 2 | 1 | 1 | Control Word Register |
| A1 | A0 | SELECTS | | | | | | | | | | | | | | | | |
| 0 | 0 | Counter 0 | | | | | | | | | | | | | | | | |
| 0 | 1 | Counter 1 | | | | | | | | | | | | | | | | |
| 1 | 0 | Counter 2 | | | | | | | | | | | | | | | | |
| 1 | 1 | Control Word Register | | | | | | | | | | | | | | | | |
| \overline{CS} | 21 | I | CHIP SELECT: A low on this input enables the 82C54 to respond to \overline{RD} and \overline{WR} signals. \overline{RD} and \overline{WR} are ignored otherwise. | | | | | | | | | | | | | | | |
| \overline{RD} | 22 | I | READ: This input is low during CPU read operations. | | | | | | | | | | | | | | | |
| \overline{WR} | 23 | I | WRITE: This input is low during CPU write operations. | | | | | | | | | | | | | | | |
| V_{CC} | 24 | | V_{CC} : The +5V power supply pin. A 0.1 μ F capacitor between pins V_{CC} and GND is recommended for decoupling. | | | | | | | | | | | | | | | |

Functional Description**General**

The 82C54 is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other computer/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This three-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 1).

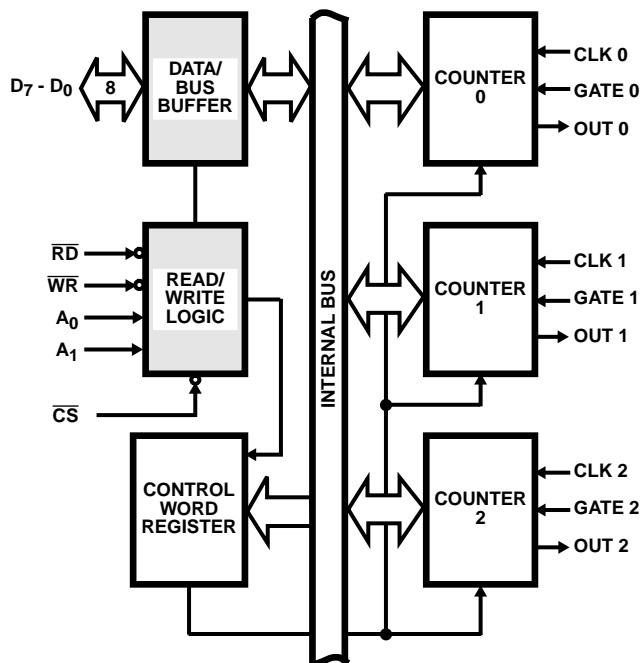


FIGURE 1. DATA BUS BUFFER AND READ/WRITE LOGIC FUNCTIONS

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the \overline{RD} input tells the 82C54 that the CPU is reading one of the counters. A "low" on the \overline{WR} input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both \overline{RD} and \overline{WR} are qualified by \overline{CS} ; \overline{RD} and \overline{WR} are ignored unless the 82C54 has been selected by holding \overline{CS} low.

Control Word Register

The Control Word Register (Figure 2) is selected by the Read/Write Logic when $A_1, A_0 = 11$. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

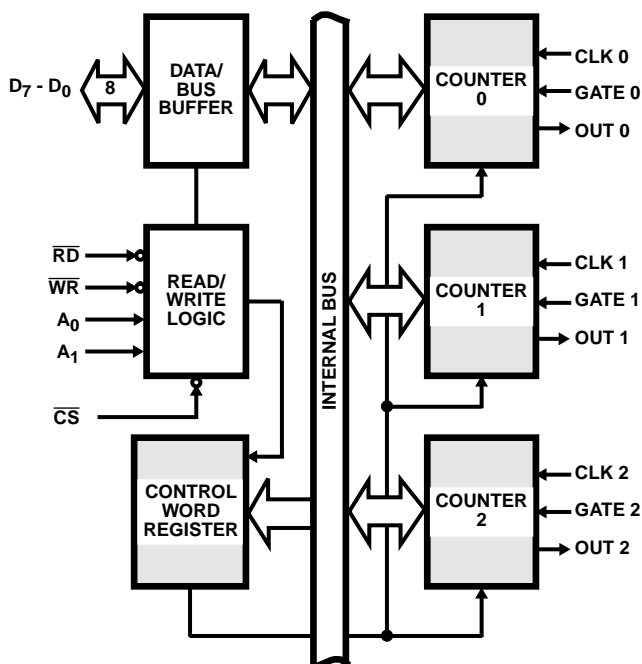


FIGURE 2. CONTROL WORD REGISTER AND COUNTER FUNCTIONS

Counter 0, Counter 1, Counter 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a signal counter is shown in Figure 3. The counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

The status register, shown in the figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labeled CE (for Counting Element). It is a 16-bit presettable synchronous down counter.

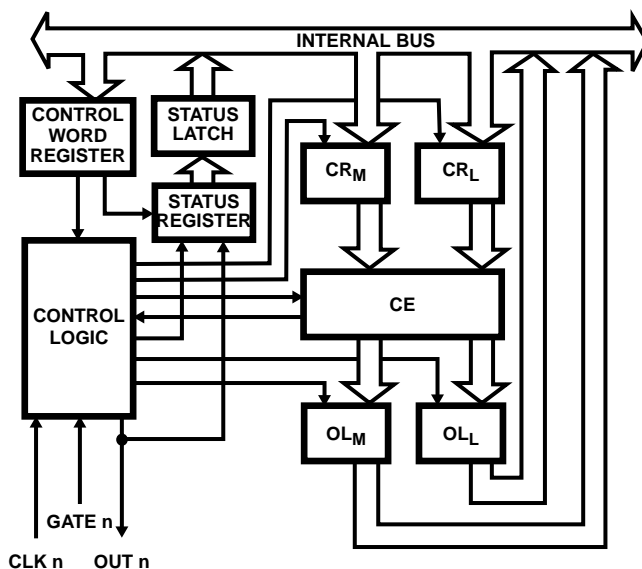


FIGURE 3. COUNTER INTERNAL BLOCK DIAGRAM

OLM and OLL are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L for "Most significant byte" and "Least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CRM and CRL (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CRM and CRL are cleared when the Counter is programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

82C54 System Interface

The 82C54 is treated by the system software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder.

Operational Description

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the 82C54

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when A1, A0 = 11. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A1, A0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

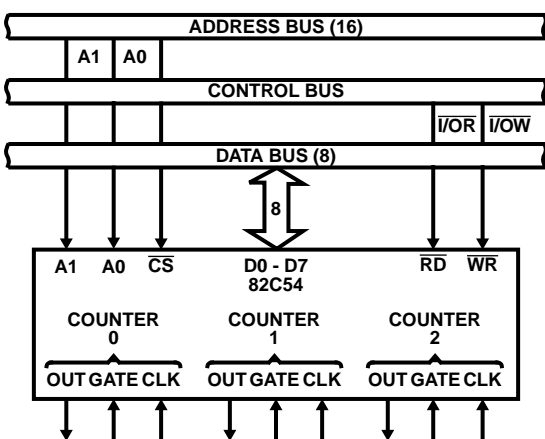


FIGURE 4. 82C54 SYSTEM INTERFACE

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1. For Each Counter, the Control Word must be written before the initial count is written.
2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A1, A0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

Control Word Format

A1, A0 = 11; \overline{CS} = 0; \overline{RD} = 1; \overline{WR} = 0

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|----|----|----|-----|
| SC1 | SC0 | RW1 | RW0 | M2 | M1 | M0 | BCD |

SC - Select Counter

| SC1 | SC0 | |
|-----|-----|---|
| 0 | 0 | Select Counter 0 |
| 0 | 1 | Select Counter 1 |
| 1 | 0 | Select Counter 2 |
| 1 | 1 | Read-Back Command (See Read Operations) |

RW - Read/Write

| RW1 | RW0 | |
|-----|-----|--|
| 0 | 0 | Counter Latch Command (See Read Operations) |
| 0 | 1 | Read/Write least significant byte only. |
| 1 | 0 | Read/Write most significant byte only. |
| 1 | 1 | Read/Write least significant byte first, then most significant byte. |

M - Mode

| M2 | M1 | M0 | |
|----|----|----|--------|
| 0 | 0 | 0 | Mode 0 |
| 0 | 0 | 1 | Mode 1 |
| X | 1 | 0 | Mode 2 |
| X | 1 | 1 | Mode 3 |
| 1 | 0 | 0 | Mode 4 |
| 1 | 0 | 1 | Mode 5 |

BCD - Binary Coded Decimal

| | |
|---|--|
| 0 | Binary Counter 16-bit |
| 1 | Binary Coded Decimal (BCD) Counter (4 Decades) |

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

Possible Programming Sequence

| | A1 | A0 |
|--------------------------|----|----|
| Control Word - Counter 0 | 1 | 1 |
| LSB of Count - Counter 0 | 0 | 0 |
| MSB of Count - Counter 0 | 0 | 0 |
| Control Word - Counter 1 | 1 | 1 |
| LSB of Count - Counter 1 | 0 | 1 |
| MSB of Count - Counter 1 | 0 | 1 |
| Control Word - Counter 2 | 1 | 1 |
| LSB of Count - Counter 2 | 1 | 0 |
| MSB of Count - Counter 2 | 1 | 0 |

Possible Programming Sequence

| | A1 | A0 |
|--------------------------|----|----|
| Control Word - Counter 0 | 1 | 1 |
| Control Word - Counter 1 | 1 | 1 |
| Control Word - Counter 2 | 1 | 1 |
| LSB of Count - Counter 2 | 1 | 0 |

Possible Programming Sequence (Continued)

| | A1 | A0 |
|--------------------------|----|----|
| LSB of Count - Counter 1 | 0 | 1 |
| LSB of Count - Counter 0 | 0 | 0 |
| MSB of Count - Counter 0 | 0 | 0 |
| MSB of Count - Counter 1 | 0 | 1 |
| MSB of Count - Counter 2 | 1 | 0 |

Possible Programming Sequence

| | A1 | A0 |
|--------------------------|----|----|
| Control Word - Counter 2 | 1 | 1 |
| Control Word - Counter 1 | 1 | 1 |
| Control Word - Counter 0 | 1 | 1 |
| LSB of Count - Counter 2 | 1 | 0 |
| MSB of Count - Counter 2 | 1 | 0 |
| LSB of Count - Counter 1 | 0 | 1 |
| MSB of Count - Counter 1 | 0 | 1 |
| LSB of Count - Counter 0 | 0 | 0 |
| MSB of Count - Counter 0 | 0 | 0 |

Possible Programming Sequence

| | A1 | A0 |
|--------------------------|----|----|
| Control Word - Counter 1 | 1 | 1 |
| Control Word - Counter 0 | 1 | 1 |
| LSB of Count - Counter 1 | 0 | 1 |
| Control Word - Counter 2 | 1 | 1 |
| LSB of Count - Counter 0 | 0 | 0 |
| MSB of Count - Counter 1 | 0 | 1 |
| LSB of Count - Counter 2 | 1 | 0 |
| MSB of Count - Counter 0 | 0 | 0 |
| MSB of Count - Counter 2 | 1 | 0 |

NOTE: In all four examples, all counters are programmed to Read/Write two-byte counts. These are only four of many programming sequences.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies. A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the Counters. The first is through the Read-Back command, which is

explained later. The second is a simple read operation of the Counter, which is selected with the A1, A0 inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

Counter Latch Command

The other method for reading the Counters involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A1, A0 = 11. Also, like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

A1, A0 = 11; $\overline{CS} = 0$; $\overline{RD} = 1$; $\overline{WR} = 0$

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|----|----|----|----|----|----|
| SC1 | SC0 | 0 | 0 | X | X | X | X |

SC1, SC0 - specify counter to be latched

| SC1 | SC0 | COUNTER |
|-----|-----|-------------------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | Read-Back Command |

D5, D4 - 00 designates Counter Latch Command, X - Don't Care.

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

The selected Counter's output latch (OL) latches the count when the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a counter is programmed to read or write two-byte counts, the following precaution applies: A program **MUST NOT** transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The read-back command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 5. The command applies to the counters selected by setting their corresponding bits D3, D2, D1 = 1.

A0, A1 = 11; $\overline{CS} = 0$; $\overline{RD} = 1$; $\overline{WR} = 0$

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|-------|--------|-------|-------|-------|----|
| 1 | 1 | COUNT | STATUS | CNT 2 | CNT 1 | CNT 0 | 0 |

- D5: 0 = Latch count of selected Counter (s)
- D4: 0 = Latch status of selected Counter(s)
- D3: 1 = Select Counter 2
- D2: 1 = Select Counter 1
- D1: 1 = Select Counter 0
- D0: Reserved for future expansion; Must be 0

FIGURE 5. READ-BACK COMMAND FORMAT

The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D5 = 0 and selecting the desired counter(s). This signal command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

| COMMANDS | | | | | | | | DESCRIPTION | RESULT |
|----------|----|----|----|----|----|----|----|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | Read-Back Count and Status of Counter 0 | Count and Status Latched for Counter 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | Read-Back Status of Counter 1 | Status Latched for Counter 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | Read-Back Status of Counters 2, 1 | Status Latched for Counter 2, But Not Counter 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | Read-Back Count of Counter 2 | Count Latched for Counter 2 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Read-Back Count and Status of Counter 1 | Count Latched for Counter 1, But Not Status |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Read-Back Status of Counter 1 | Command Ignored, Status Already Latched for Counter 1 |

FIGURE 7. READ-BACK COMMAND EXAMPLE

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 6. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------|------------|-----|-----|----|----|----|-----|
| OUTPUT | NULL COUNT | RW1 | RW0 | M2 | M1 | M0 | BCD |

- D7: 1 = Out pin is 1
0 = Out pin is 0
- D6: 1 = Null count
0 = Count available for reading
- D5 - D0 = Counter programmed mode (See Control Word Formats)

FIGURE 6. STATUS BYTE

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the counter is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown below.

THIS ACTION: CAUSES:

- A. Write to the control word register:(1) Null Count = 1
 - B. Write to the count register (CR):(2) Null Count = 1
 - C. New count is loaded into CE (CR - CE) Null Count = 0
- (1) Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.
- (2) If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D5, D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 7.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

| CS | RD | WR | A1 | A0 | |
|----|----|----|----|----|----------------------------|
| 0 | 1 | 0 | 0 | 0 | Write into Counter 0 |
| 0 | 1 | 0 | 0 | 1 | Write into Counter 1 |
| 0 | 1 | 0 | 1 | 0 | Write into Counter 2 |
| 0 | 1 | 0 | 1 | 1 | Write Control Word |
| 0 | 0 | 1 | 0 | 0 | Read from Counter 0 |
| 0 | 0 | 1 | 0 | 1 | Read from Counter 1 |
| 0 | 0 | 1 | 1 | 0 | Read from Counter 2 |
| 0 | 0 | 1 | 1 | 1 | No-Operation (Three-State) |
| 1 | X | X | X | X | No-Operation (Three-State) |
| 0 | 1 | 1 | X | X | No-Operation (Three-State) |

FIGURE 8. READ/WRITE OPERATIONS SUMMARY

Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE:

A rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER:

A rising edge of a Counter's Gate input.

COUNTER LOADING:

The transfer of a count from the CR to the CE (See "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

- (1) Writing the first byte disables counting. Out is set low immediately (no clock pulse required).
- (2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the counter as this has already been done.

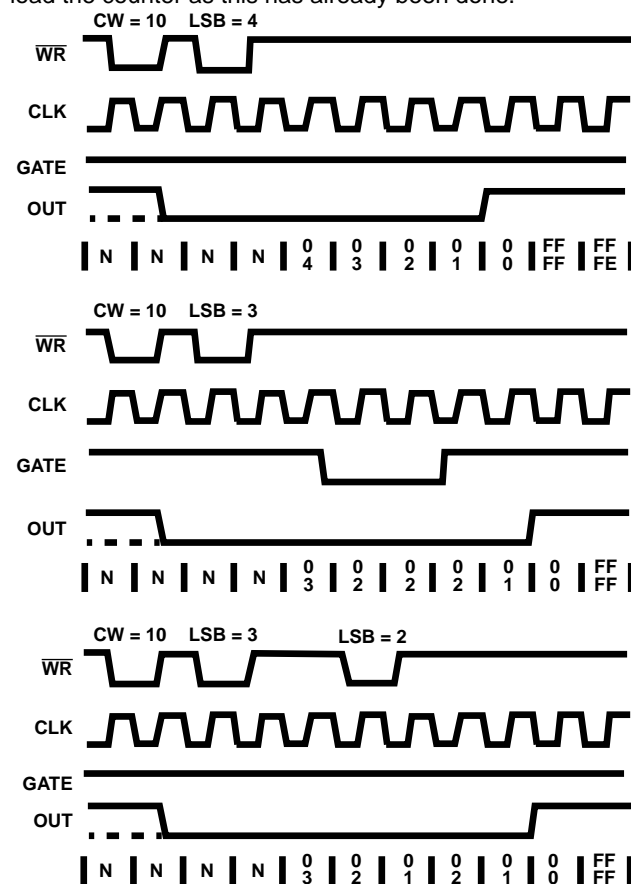


FIGURE 9. MODE 0

NOTES: The following conventions apply to all mode timing diagrams.

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected (\overline{CS} always low).
3. CW stands for "Control Word"; CW = 10 means a control word of 10, Hex is written to the counter.
4. LSB stands for Least significant "byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

Mode 1: Hardware Retriggerable One-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggerable. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

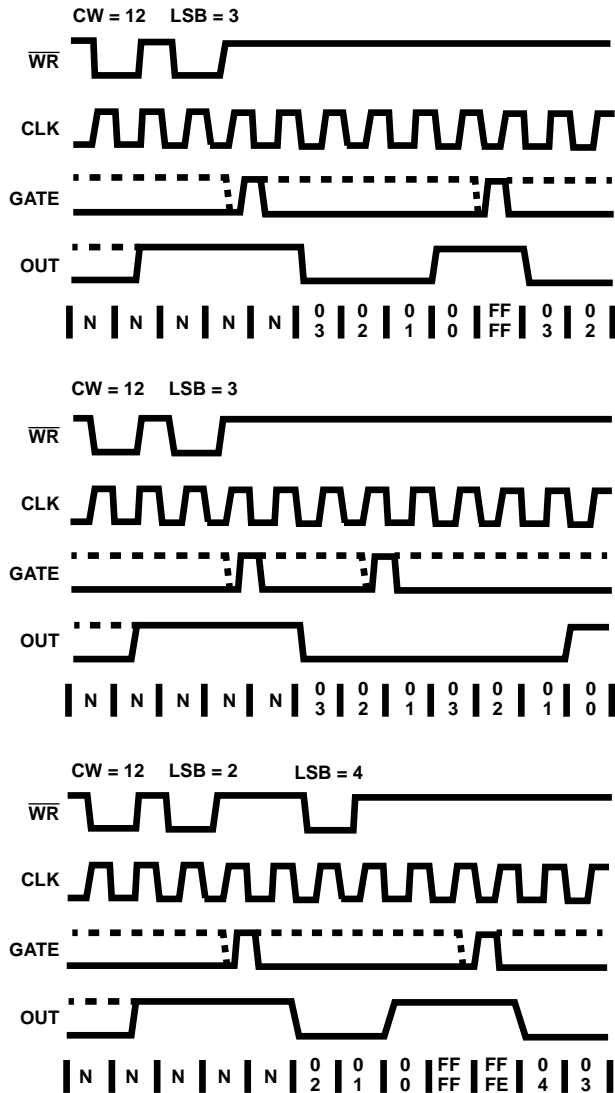


FIGURE 10. MODE 1

Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock Interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the end of the current counting cycle.

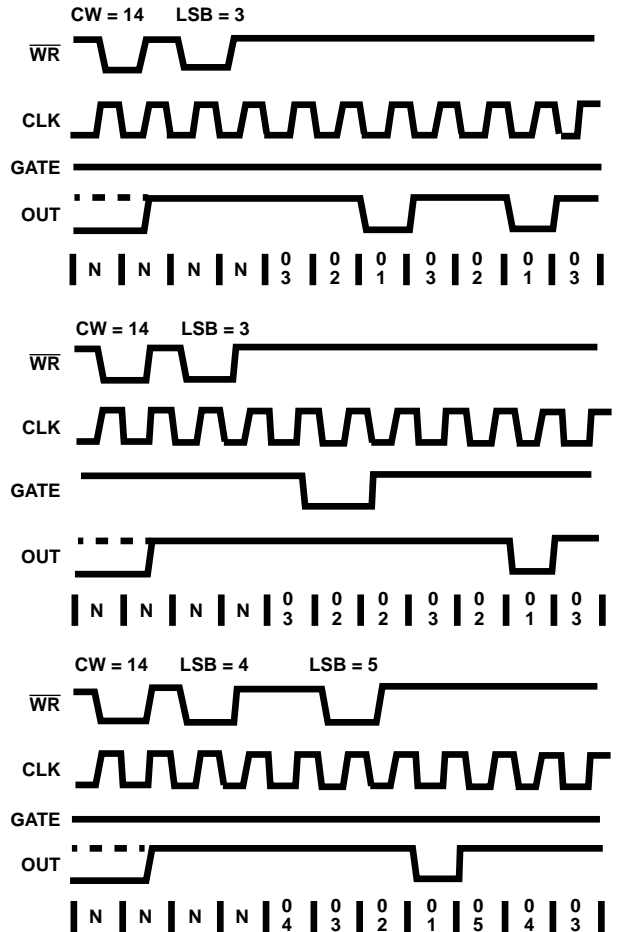


FIGURE 11. MODE 2

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

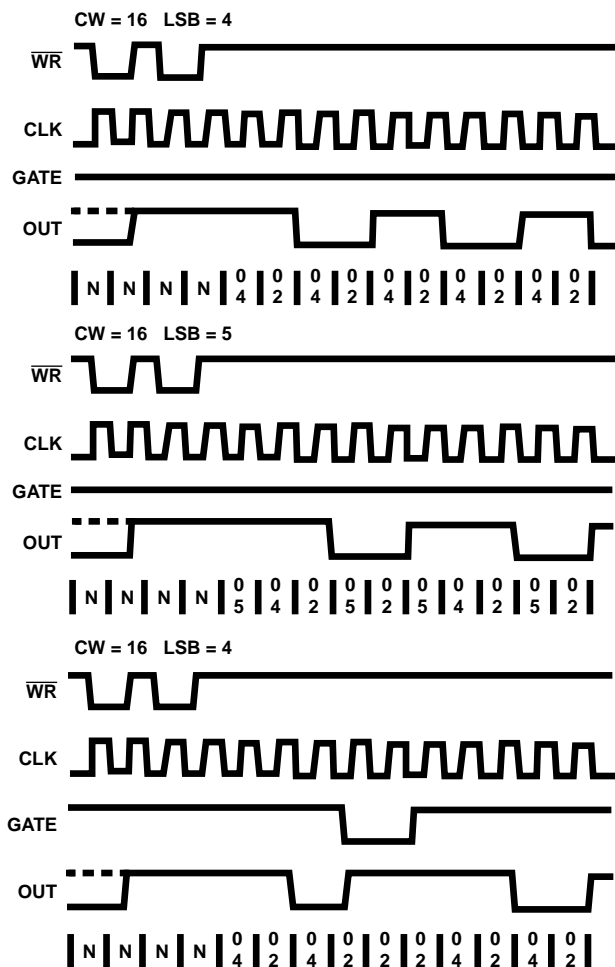


FIGURE 12. MODE 3

Mode 3 is Implemented as Follows:

EVEN COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

ODD COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse, decremented by one on the next CLK pulse, and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the Counter is reloaded with the initial count. The count is decremented by three on the next CLK pulse, and then by two on succeeding CLK pulses. When the count expires, OUT goes high again and the Counter is reloaded with the initial count. The above process is repeated indefinitely. So for odd counts, OUT will be high for $(N + 1)/2$ counts and low for $(N - 1)/2$ counts.

Mode 4: Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse then go high again. The counting sequence is "Triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

- (1) Writing the first byte has no effect on counting.
- (2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobos low N + 1 CLK pulses after the new count of N is written.

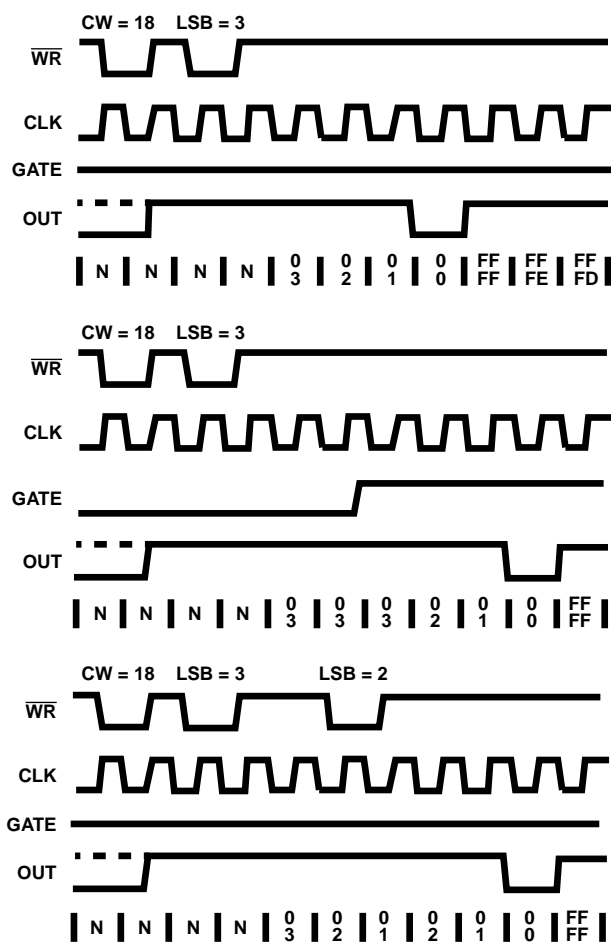


FIGURE 13. MODE 4

Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is triggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with new count on the next CLK pulse and counting will continue from there.

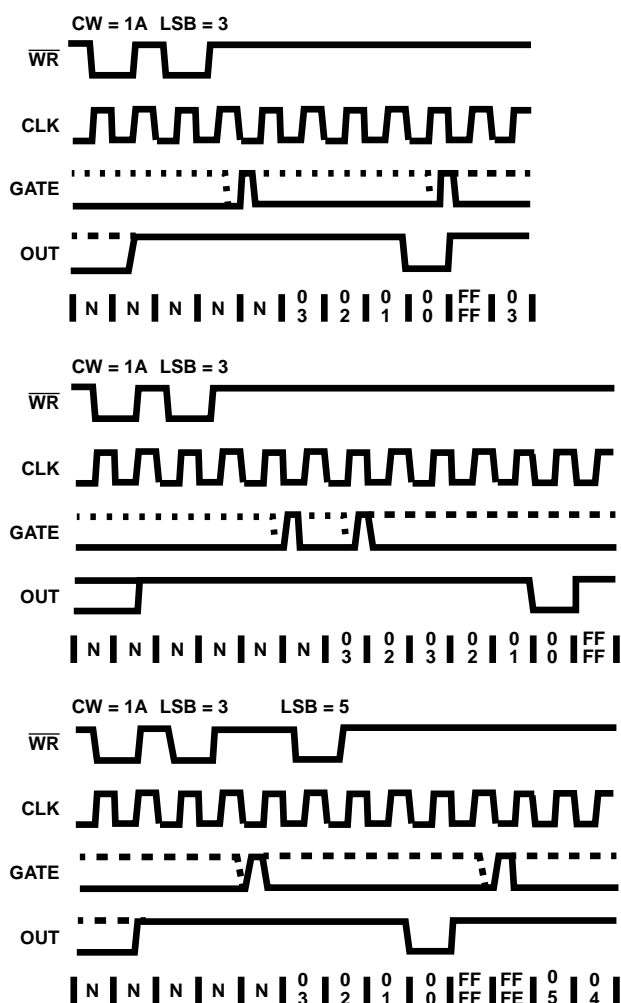


FIGURE 14. MODE 5

Operation Common to All Modes**Programming**

When a Control Word is written to a Counter, all Control Logic, is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3 and 4 the GATE input is level sensitive, and logic level is sampled on the rising edge of CLK. In modes 1, 2, 3 and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of Gate (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK. The flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs - a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive.

Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

| SIGNAL STATUS MODES | LOW OR GOING LOW | RISING | HIGH |
|---------------------|---|--|------------------|
| 0 | Disables Counting | - | Enables Counting |
| 1 | - | 1) Initiates Counting 2) Resets output after next clock | - |
| 2 | 1) Disables counting 2) Sets output immediately high | Initiates Counting | Enables Counting |
| 3 | 1) Disables counting 2) Sets output immediately high | Initiates Counting | Enables Counting |
| 4 | 1) Disables Counting | - | Enables Counting |
| 5 | - | Initiates Counting | - |

FIGURE 15. GATE PIN OPERATIONS SUMMARY

| MODE | MIN COUNT | MAX COUNT |
|------|-----------|-----------|
| 0 | 1 | 0 |
| 1 | 1 | 0 |
| 2 | 2 | 0 |
| 3 | 2 | 0 |
| 4 | 1 | 0 |
| 5 | 1 | 0 |

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

FIGURE 16. MINIMUM AND MAXIMUM INITIAL COUNTS

CMOS Programmable Peripheral Interface

June 1998

Features

- Pin Compatible with NMOS 8255A
- 24 Programmable I/O Pins
- Fully TTL Compatible
- High Speed, No "Wait State" Operation with 5MHz and 8MHz 80C86 and 80C88
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- L7 Process
- 2.5mA Drive Capability on All I/O Ports
- Low Standby Power (ICCSB)10 μ A

Description

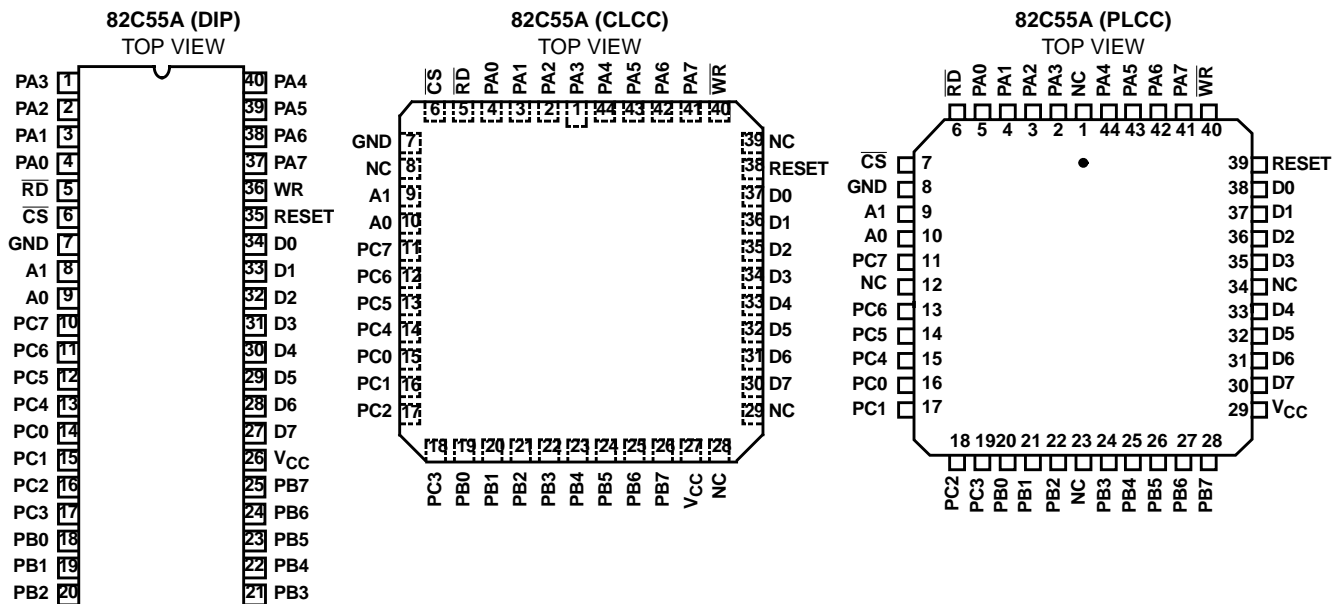
The Intersil 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with the 80C86, 80C88 and other microprocessors.

Static CMOS circuit design insures low operating power. TTL compatibility over the full military temperature range and bus hold circuitry eliminate the need for pull-up resistors. The Intersil advanced SAJI process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power.

Ordering Information

| PART NUMBERS | | PACKAGE | TEMPERATURE RANGE | PKG. NO. |
|--------------|------------|--------------|-------------------|----------|
| 5MHz | 8MHz | | | |
| CP82C55A-5 | CP82C55A | 40 Ld PDIP | 0°C to 70°C | E40.6 |
| IP82C55A-5 | IP82C55A | | -40°C to 85°C | E40.6 |
| CS82C55A-5 | CS82C55A | 44 Ld PLCC | 0°C to 70°C | N44.65 |
| IS82C55A-5 | IS82C55A | | -40°C to 85°C | N44.65 |
| CD82C55A-5 | CD82C55A | 40 Ld CERDIP | 0°C to 70°C | F40.6 |
| ID82C55A-5 | ID82C55A | | -40°C to 85°C | F40.6 |
| MD82C55A-5/B | MD82C55A/B | | -55°C to 125°C | F40.6 |
| 8406601QA | 8406602QA | | SMD# | F40.6 |
| MR82C55A-5/B | MR82C55A/B | 44 Pad CLCC | -55°C to 125°C | J44.A |
| 8406601XA | 8406602XA | | SMD# | J44.A |

Pinouts

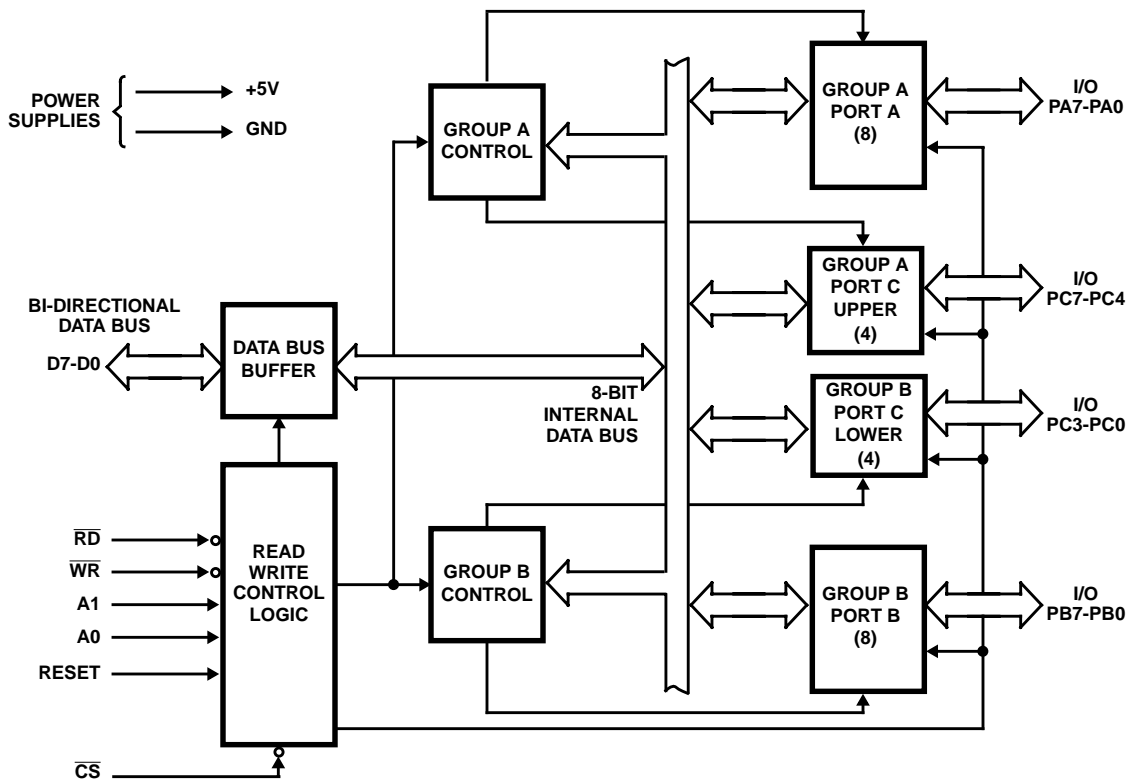


82C55A

Pin Description

| SYMBOL | PIN NUMBER | TYPE | DESCRIPTION |
|-----------------|------------|------|---|
| V _{CC} | 26 | | V _{CC} : The +5V power supply pin. A 0.1μF capacitor between pins 26 and 7 is recommended for decoupling. |
| GND | 7 | | GROUND |
| D0-D7 | 27-34 | I/O | DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus. |
| RESET | 35 | I | RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on. |
| \overline{CS} | 6 | I | CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications. |
| \overline{RD} | 5 | I | READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus. |
| \overline{WR} | 36 | I | WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A. |
| A0-A1 | 8, 9 | I | ADDRESS: These input signals, in conjunction with the \overline{RD} and \overline{WR} inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1. |
| PA0-PA7 | 1-4, 37-40 | I/O | PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port. |
| PB0-PB7 | 18-25 | I/O | PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port. |
| PC0-PC7 | 10-17 | I/O | PORT C: 8-bit input and output port. Bus hold circuitry is present on this port. |

Functional Diagram



Functional Description

Data Bus Buffer

This three-state bi-directional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS) Chip Select. A “low” on this input pin enables the communication between the 82C55A and the CPU.

(RD) Read. A “low” on this input pin enables 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to “read from” the 82C55A.

(WR) Write. A “low” on this input pin enables the CPU to write data or control words into the 82C55A.

(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

82C55A BASIC OPERATION

| A1 | A0 | RD | WR | CS | INPUT OPERATION (READ) |
|--------------------------|----|----|----|----|-------------------------|
| 0 | 0 | 0 | 1 | 0 | Port A → Data Bus |
| 0 | 1 | 0 | 1 | 0 | Port B → Data Bus |
| 1 | 0 | 0 | 1 | 0 | Port C → Data Bus |
| 1 | 1 | 0 | 1 | 0 | Control Word → Data Bus |
| OUTPUT OPERATION (WRITE) | | | | | |
| 0 | 0 | 1 | 0 | 0 | Data Bus → Port A |
| 0 | 1 | 1 | 0 | 0 | Data Bus → Port B |
| 1 | 0 | 1 | 0 | 0 | Data Bus → Port C |
| 1 | 1 | 1 | 0 | 0 | Data Bus → Control |
| DISABLE FUNCTION | | | | | |
| X | X | X | X | 1 | Data Bus → Three-State |
| X | X | 1 | 1 | 0 | Data Bus → Three-State |

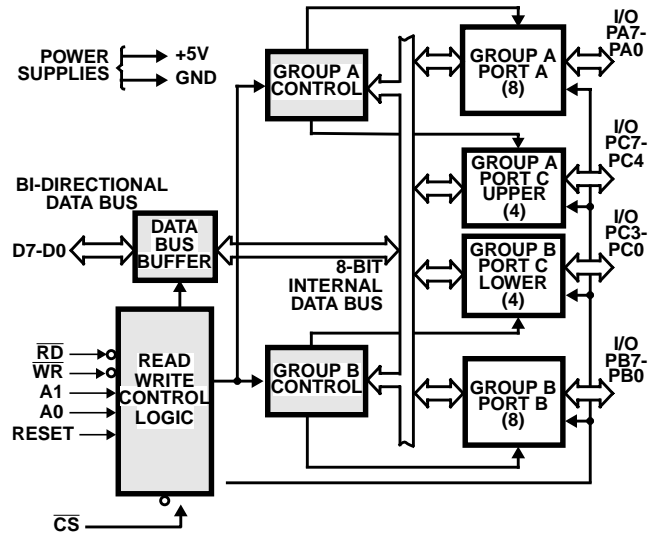


FIGURE 1. 82C55A BLOCK DIAGRAM. DATA BUS BUFFER, READ/WRITE, GROUP A & B CONTROL LOGIC FUNCTIONS

(RESET) Reset. A “high” on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode. “Bus hold” devices internal to the 82C55A will hold the I/O port inputs to a logic “1” state with a maximum hold current of 400µA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU “outputs” a control word to the 82C55A. The control word contains information such as “mode”, “bit set”, “bit reset”, etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts “commands” from the Read/Write Control logic, receives “control words” from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)

Control Group B - Port B and Port C lower (C3 - C0)

The control word register can be both written and read as shown in the “Basic Operation” table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic “1”, as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A. See Figure 2A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B. See Figure 2B.

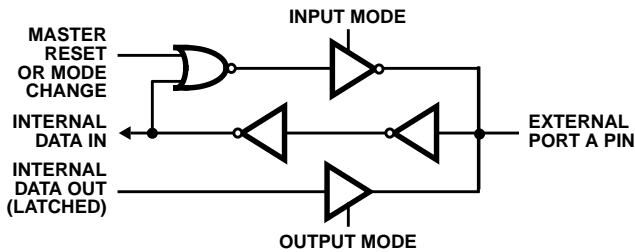


FIGURE 2A. PORT A BUS-HOLD CONFIGURATION

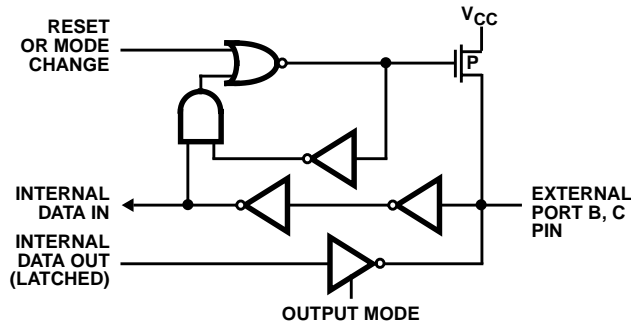


FIGURE 2B. PORT B AND C BUS-HOLD CONFIGURATION

FIGURE 2. BUS-HOLD CONFIGURATION

Operational Description

Mode Selection

There are three basic modes of operation that can be selected by the system software:

- Mode 0 - Basic Input/Output
- Mode 1 - Strobed Input/Output
- Mode 2 - Bi-directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need to pullup or pull-down resistors in all-CMOS designs. The control word

register will contain 9Bh. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine. Any port programmed as an output port is initialized to all zeros when the control word is written.

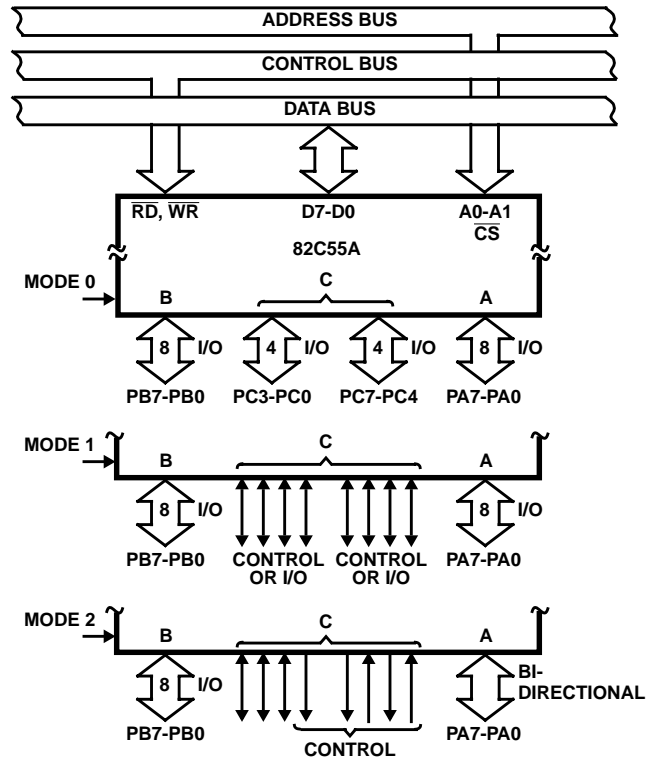


FIGURE 3. BASIC MODE DEFINITIONS AND BUS INTERFACE

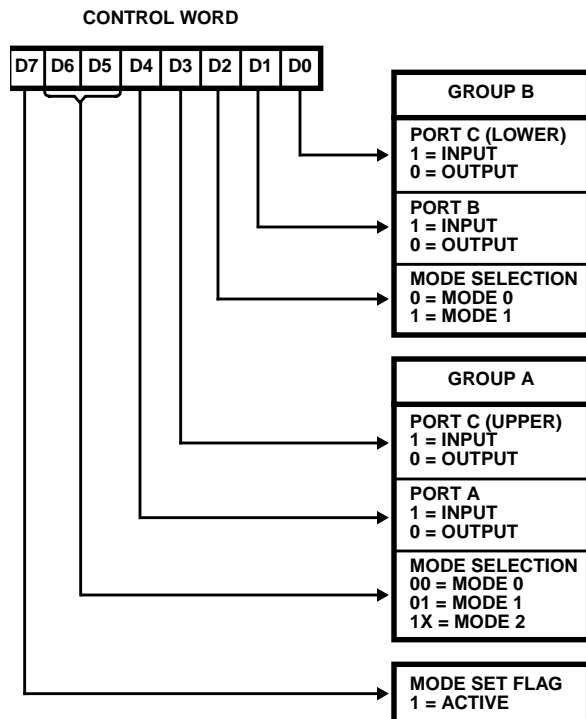


FIGURE 4. MODE DEFINITION FORMAT

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first, but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs. PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature (Figure 5)

Any of the eight bits of Port C can be Set or Reset using a single Output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were output ports.

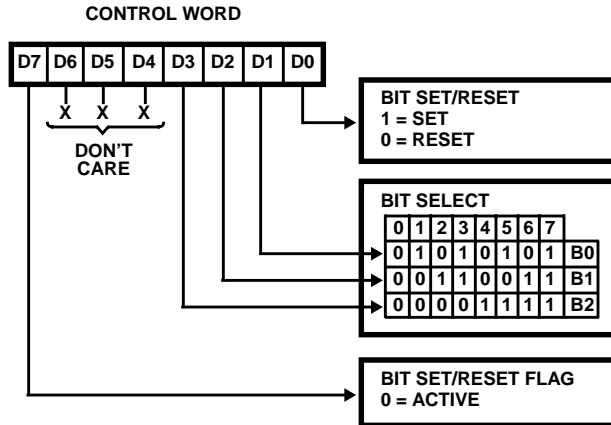


FIGURE 5. BIT SET/RESET FORMAT

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition

(BIT-SET)-INTE is SET - Interrupt Enable

(BIT-RESET)-INTE is Reset - Interrupt Disable

NOTE: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

Mode 0 Basic Functional Definitions:

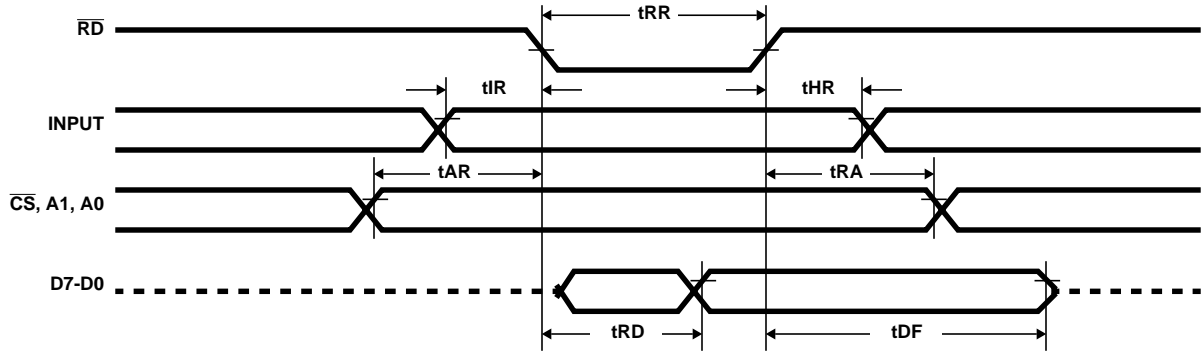
- Two 8-bit ports and two 4-bit ports
- Any Port can be input or output
- Outputs are latched
- Input are not latched
- 16 different Input/Output configurations possible

MODE 0 PORT DEFINITION

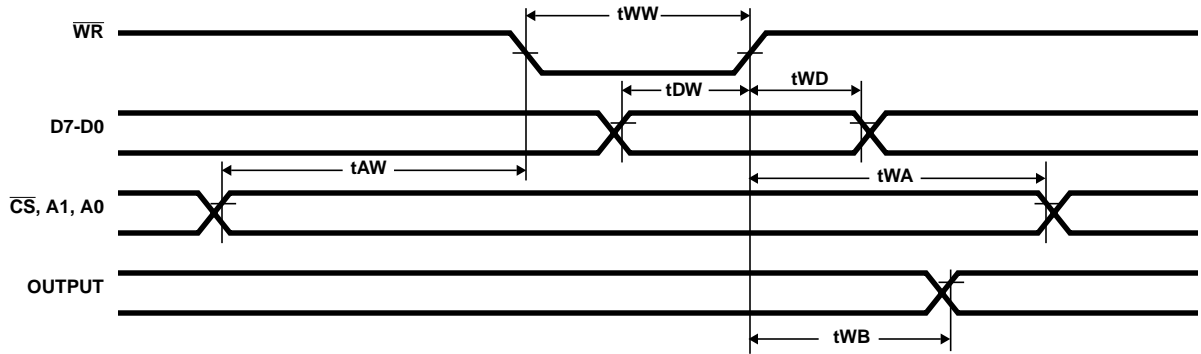
| A | | B | | GROUP A | | # | GROUP B | |
|----|----|----|----|---------|---------------|----|---------|---------------|
| D4 | D3 | D1 | D0 | PORT A | PORTC (Upper) | | PORT B | PORTC (Lower) |
| 0 | 0 | 0 | 0 | Output | Output | 0 | Output | Output |
| 0 | 0 | 0 | 1 | Output | Output | 1 | Output | Input |
| 0 | 0 | 1 | 0 | Output | Output | 2 | Input | Output |
| 0 | 0 | 1 | 1 | Output | Output | 3 | Input | Input |
| 0 | 1 | 0 | 0 | Output | Input | 4 | Output | Output |
| 0 | 1 | 0 | 1 | Output | Input | 5 | Output | Input |
| 0 | 1 | 1 | 0 | Output | Input | 6 | Input | Output |
| 0 | 1 | 1 | 1 | Output | Input | 7 | Input | Input |
| 1 | 0 | 0 | 0 | Input | Output | 8 | Output | Output |
| 1 | 0 | 0 | 1 | Input | Output | 9 | Output | Input |
| 1 | 0 | 1 | 0 | Input | Output | 10 | Input | Output |
| 1 | 0 | 1 | 1 | Input | Output | 11 | Input | Input |
| 1 | 1 | 0 | 0 | Input | Input | 12 | Output | Output |
| 1 | 1 | 0 | 1 | Input | Input | 13 | Output | Input |
| 1 | 1 | 1 | 0 | Input | Input | 14 | Input | Output |
| 1 | 1 | 1 | 1 | Input | Input | 15 | Input | Input |

82C55A

Mode 0 (Basic Input)



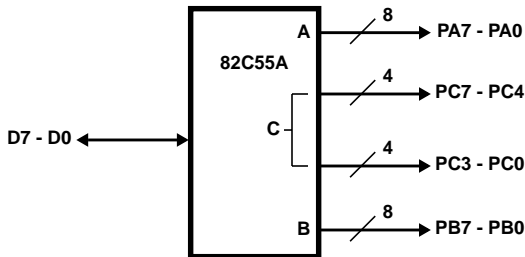
Mode 0 (Basic Output)



Mode 0 Configurations

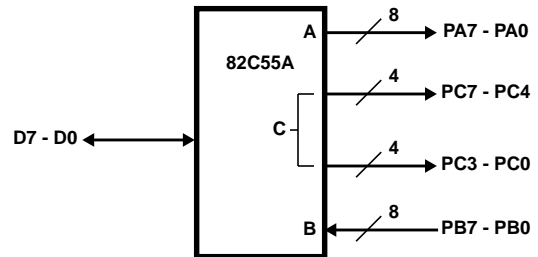
CONTROL WORD #0

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |



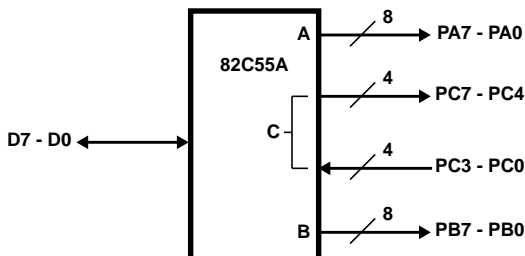
CONTROL WORD #2

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |



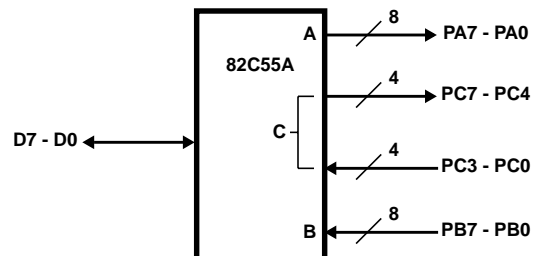
CONTROL WORD #1

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |



CONTROL WORD #3

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

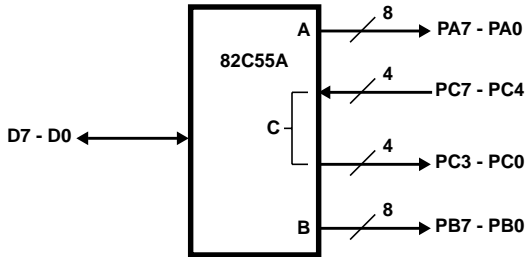


82C55A

Mode 0 Configurations (Continued)

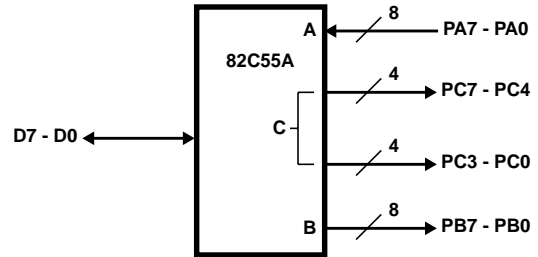
CONTROL WORD #4

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |



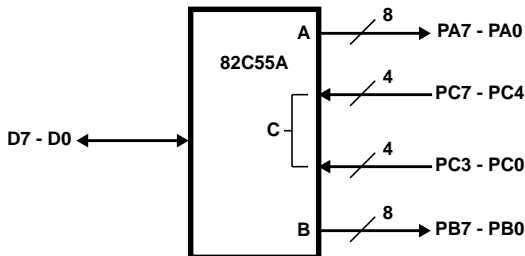
CONTROL WORD #8

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |



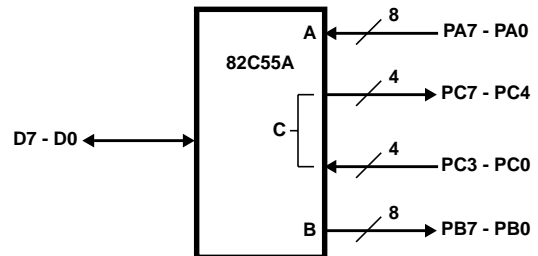
CONTROL WORD #5

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |



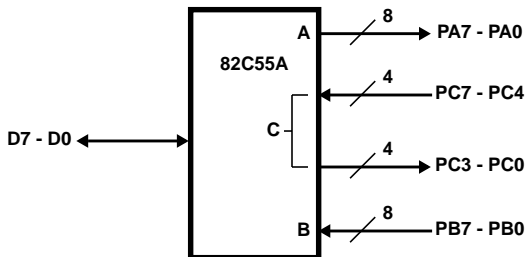
CONTROL WORD #9

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |



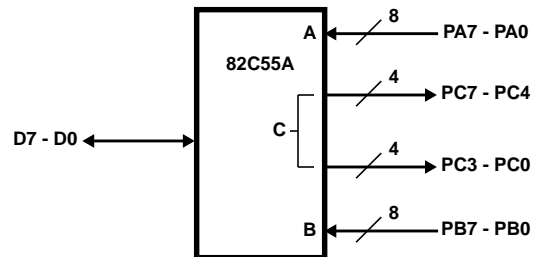
CONTROL WORD #6

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |



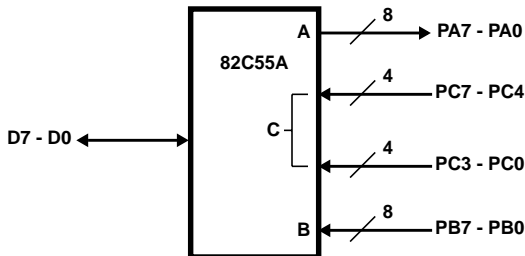
CONTROL WORD #10

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |



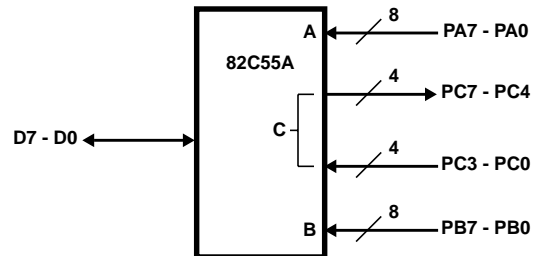
CONTROL WORD #7

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |



CONTROL WORD #11

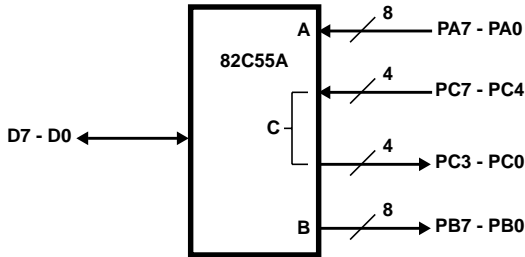
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |



Mode 0 Configurations (Continued)

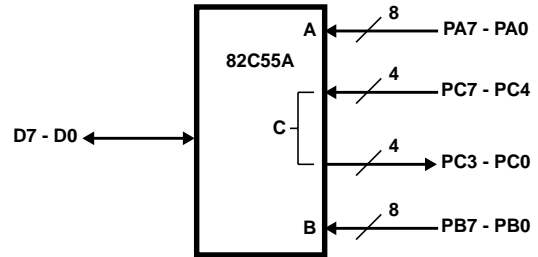
CONTROL WORD #12

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |



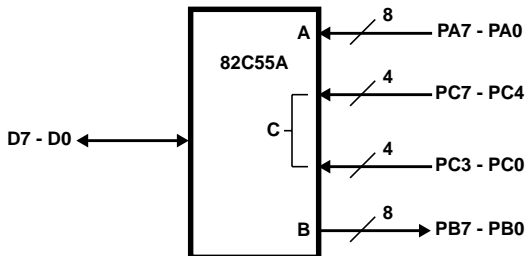
CONTROL WORD #14

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |



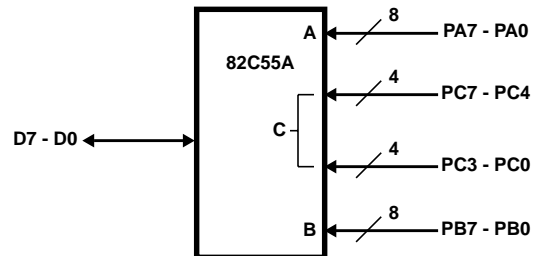
CONTROL WORD #13

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |



CONTROL WORD #15

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |



Operating Modes

Mode 1 - (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "hand shaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "hand shaking" signals.

Mode 1 Basic Function Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

(Figures 6 and 7)

STB (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch: in essence, and acknowledgment. IBF is set by \overline{STB} input being low and is reset by the rising edge of the \overline{RD} input.

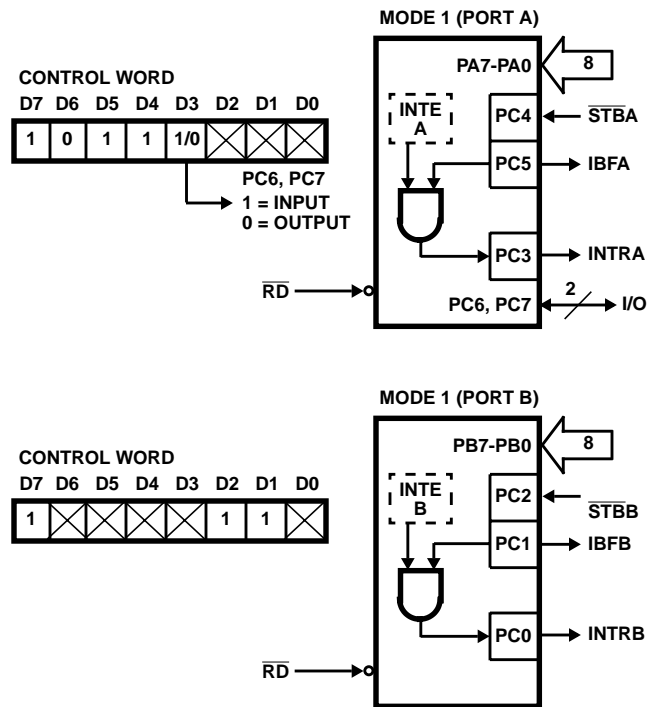


FIGURE 6. MODE 1 INPUT

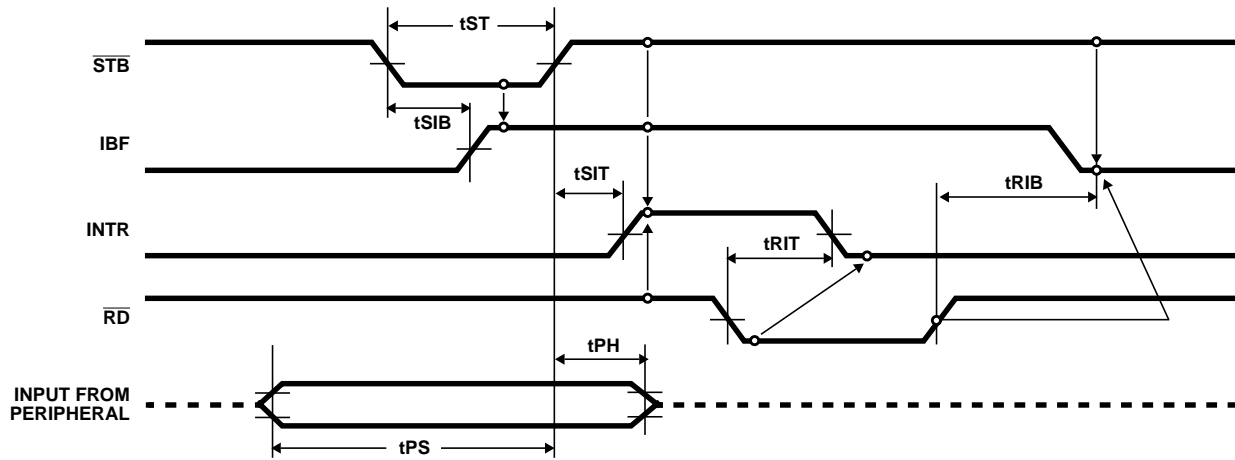


FIGURE 7. MODE 1 (STROBED INPUT)

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. \overline{INTR} is set by the condition: \overline{STB} is a "one", \overline{IBF} is a "one" and \overline{INTE} is a "one". It is reset by the falling edge of \overline{RD} . This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Output Control Signal Definition

(Figure 8 and 9)

\overline{OBF} - Output Buffer Full F/F. The \overline{OBF} output will go "low" to indicate that the CPU has written data out to be specified port. This does not mean valid data is sent out of the port at this time since \overline{OBF} can go true before data is available. Data is guaranteed valid at the rising edge of \overline{OBF} , (See Note 1). The \overline{OBF} F/F will be set by the rising edge of the \overline{WR} input and reset by \overline{ACK} input being low.

\overline{ACK} - Acknowledge Input. A "low" on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data, (See Note 1).

INTR - (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. \overline{INTR} is set when \overline{ACK} is a "one", \overline{OBF} is a "one" and \overline{INTE} is a "one". It is reset by the falling edge of \overline{WR} .

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

NOTE:

1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send \overline{OBF} to the peripheral device, generates an \overline{ACK} from the peripheral device and then latch data into the peripheral device on the rising edge of \overline{OBF} .

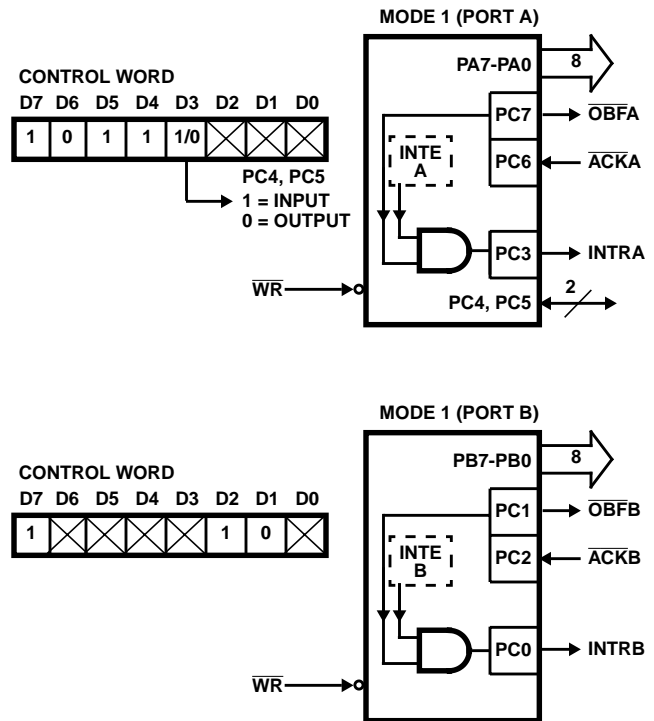


FIGURE 8. MODE 1 OUTPUT

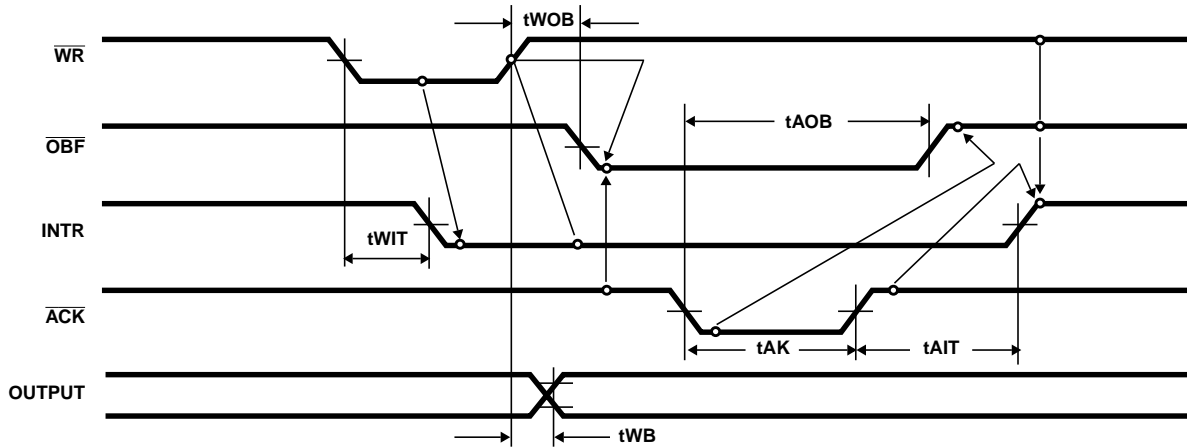


FIGURE 9. MODE 1 (STROBED OUTPUT)

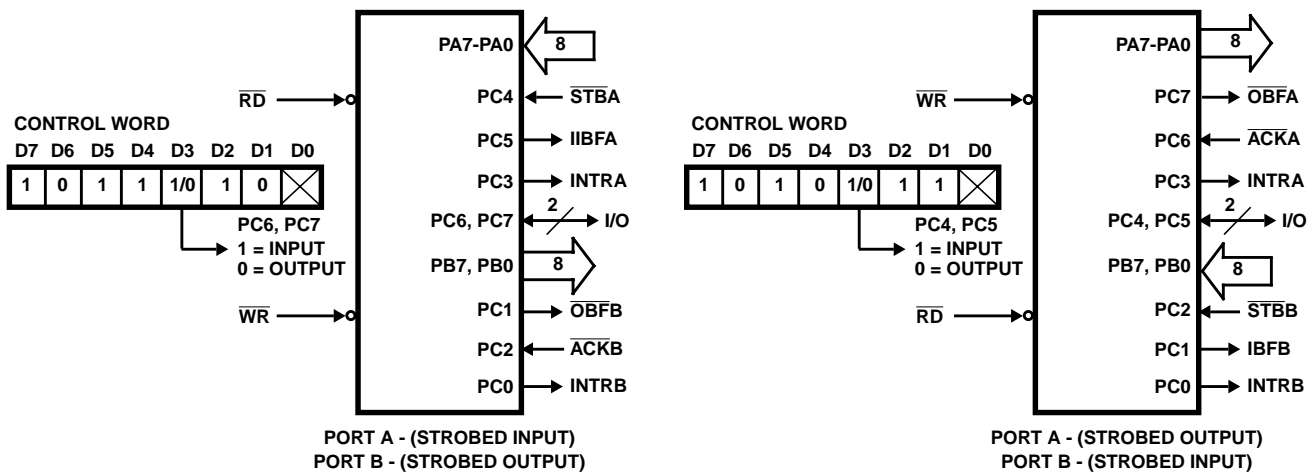


FIGURE 10. COMBINATIONS OF MODE 1

Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Hand shaking" signals are provided to maintain proper bus flow discipline similar to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C)
- Both inputs and outputs are latched
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

Bi-Directional Bus I/O Control Signal Definition

(Figures 11, 12, 13, 14)

INTR - (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

OBF - (Output Buffer Full). The $\overline{\text{OBF}}$ output will go "low" to indicate that the CPU has written data out to port A.

ACK - (Acknowledge). A "low" on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 - (The INTE flip-flop associated with $\overline{\text{OBF}}$). Controlled by bit set/reset of PC4.

Input Operations

STB - (Strobe Input). A "low" on this input loads data into the input latch.

IBF - (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 - (The INTE flip-flop associated with IBF). Controlled by bit set/reset of PC4.

82C55A

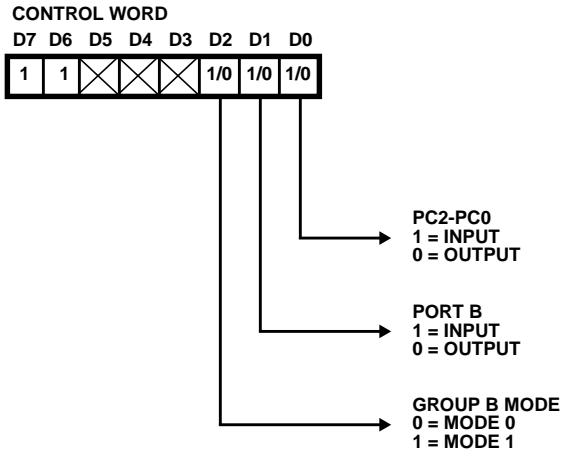


FIGURE 11. MODE CONTROL WORD

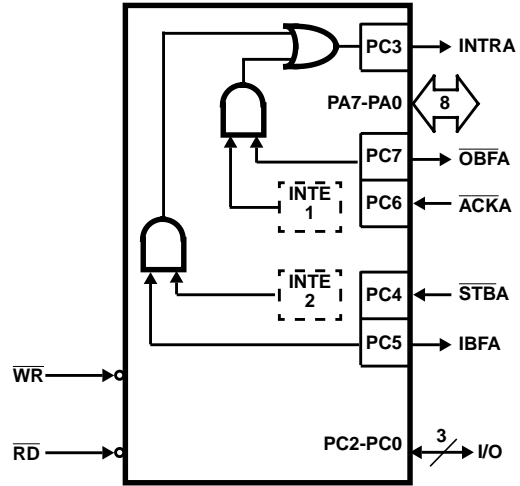
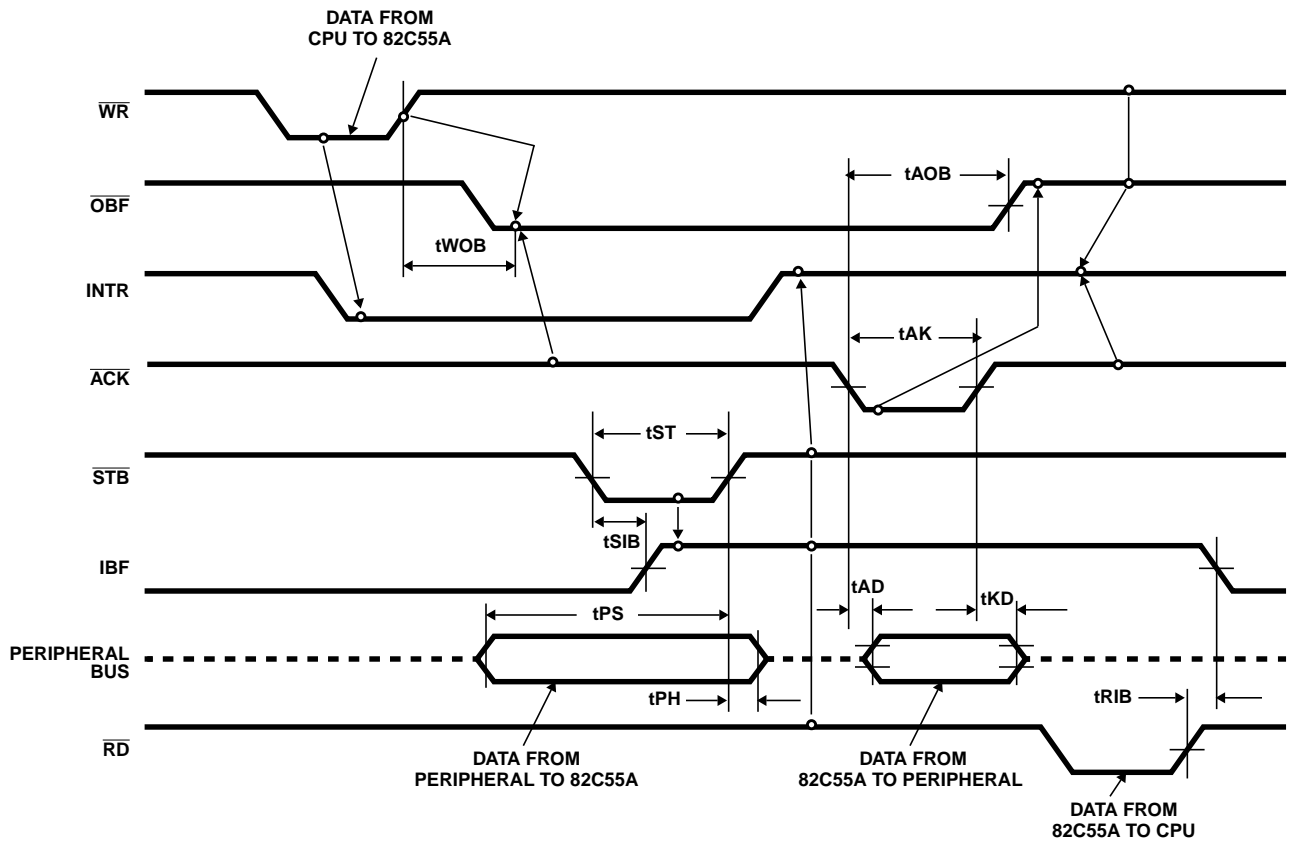


FIGURE 12. MODE 2

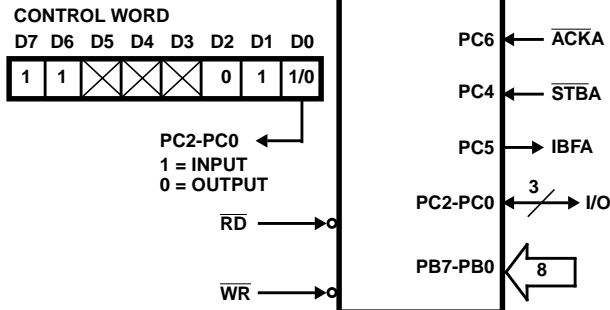


NOTE: Any sequence where \overline{WR} occurs before \overline{ACK} and \overline{STB} occurs before RD is permissible. ($INTR = IBF \cdot MASK \cdot \overline{STB} \cdot \overline{RD} \div \overline{OBF} \cdot MASK \cdot \overline{ACK} \cdot \overline{WR}$)

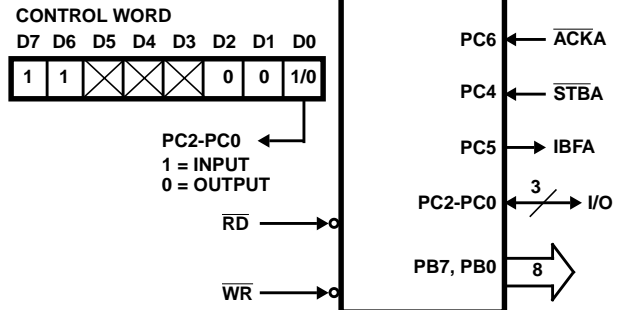
FIGURE 13. MODE 2 (BI-DIRECTIONAL)

82C55A

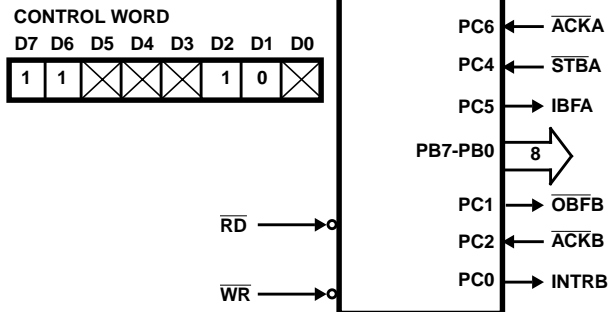
MODE 2 AND MODE 0 (INPUT)



MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)

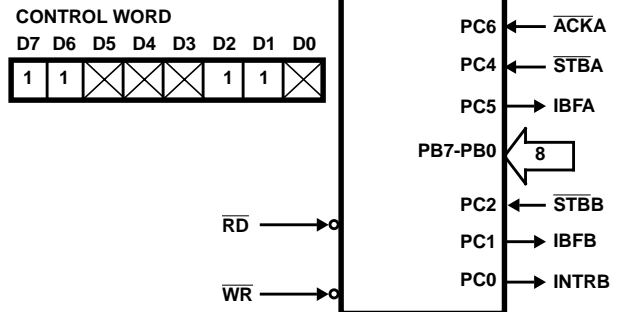


FIGURE 14. MODE 2 COMBINATIONS

MODE DEFINITION SUMMARY

| | MODE 0 | | MODE 1 | | MODE 2 |
|-----|--------|-----|--------|-------|-------------------------|
| | IN | OUT | IN | OUT | GROUP A ONLY |
| PA0 | In | Out | In | Out | ↔ |
| PA1 | In | Out | In | Out | ↔ |
| PA2 | In | Out | In | Out | ↔ |
| PA3 | In | Out | In | Out | ↔ |
| PA4 | In | Out | In | Out | ↔ |
| PA5 | In | Out | In | Out | ↔ |
| PA6 | In | Out | In | Out | ↔ |
| PA7 | In | Out | In | Out | ↔ |
| PB0 | In | Out | In | Out | } Mode 0 or Mode 1 Only |
| PB1 | In | Out | In | Out | |
| PB2 | In | Out | In | Out | |
| PB3 | In | Out | In | Out | |
| PB4 | In | Out | In | Out | |
| PB5 | In | Out | In | Out | |
| PB6 | In | Out | In | Out | |
| PB7 | In | Out | In | Out | |
| PC0 | In | Out | INTRB | INTRB | I/O |
| PC1 | In | Out | IBFB | OBFB | I/O |
| PC2 | In | Out | STBB | ACKB | I/O |
| PC3 | In | Out | INTRA | INTRA | INTRA |
| PC4 | In | Out | STBA | I/O | STBA |
| PC5 | In | Out | IBFA | I/O | IBFA |
| PC6 | In | Out | I/O | ACKA | ACKA |
| PC7 | In | Out | I/O | OBFA | OBFA |

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the \overline{ACK} and \overline{STB} lines, will be placed on the data bus. In place of the \overline{ACK} and \overline{STB} line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port Cea Bit" command, any Port C line programmed as an output (including IBF and \overline{OB}) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including \overline{ACK} and \overline{STB} lines, associated with Port C fare not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the \overline{ACK} and \overline{STB} lines with the "Set Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

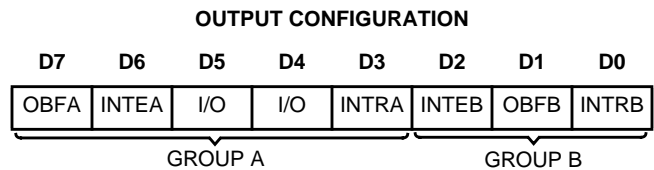
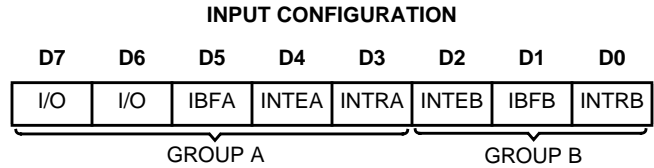


FIGURE 15. MODE 1 STATUS WORD FORMAT

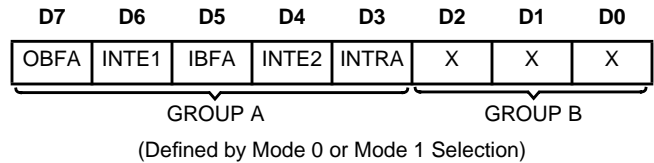


FIGURE 16. MODE 2 STATUS WORD FORMAT

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status (Figures 15 and 16)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is not special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

| INTERRUPT ENABLE FLAG | POSITION | ALTERNATE PORT C PIN SIGNAL (MODE) |
|-----------------------|----------|---|
| INTE B | PC2 | \overline{ACKB} (Output Mode 1) or \overline{STBB} (Input Mode 1) |
| INTE A2 | PC4 | \overline{STBA} (Input Mode 1 or Mode 2) |
| INTE A1 | PC6 | \overline{ACKA} (Output Mode 1 or Mode 2) |

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Applications of the 82C55A

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly "fit" the application. Figures 18 through 24 present a few examples of typical applications of the 82C55A.

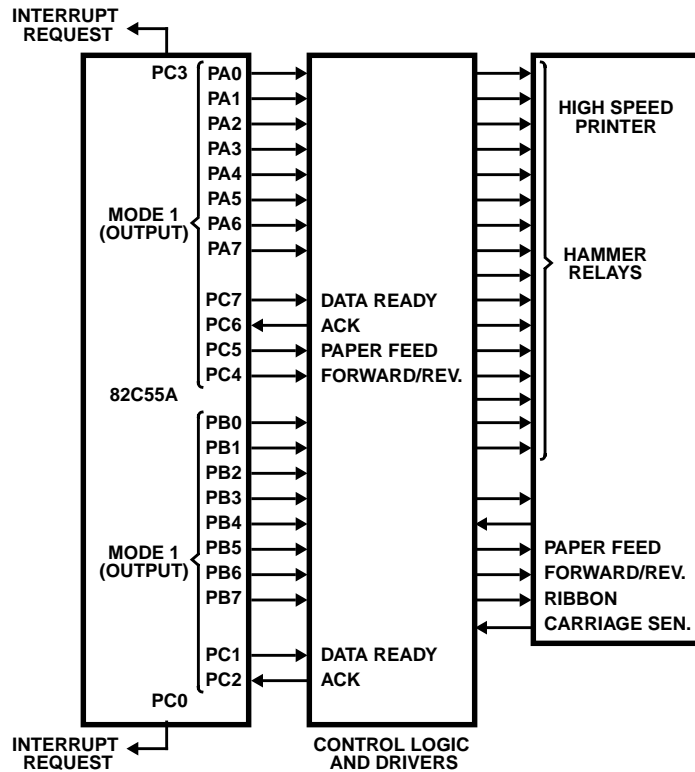


FIGURE 18. PRINTER INTERFACE